**Report joint workshop on NGTCCD**
**Garching 9-22 Nov 2006**

**Peter Sinclaire (La Silla) & Philippe Duhoux (Garching)**

# 1 - Purpose of mission

This mission was aimed to solve most of the pending problems encountered during the previous months while deploying the new systems on the La Silla telescopes.
Especially there were following problems:

1. Spurious horizontal jitter on CCD47-20 in window mode
2. Spurious garbage lines in 2 window readout CCD57
3. Horizontal binning by 4 incorrect on CCD57
4. Binning and windowing not fully implemented on CCD47

In addition, 5 systems had to be delivered:

1. X-Shooter [1 system with Thick Head CCD57]
2. PRIMA/STS (APE/PYPS) [1 system with Thick Head CCD57]
3. UVES Upgrade [3 systems with Thin Heads CCD57]

And last, 6 heads had to be assembled and tested.

# 2 - Results

The mission went smoothly although we had to face the problem related to the recently upgraded controllers.

## *2.1 - Hardware*

### 2.1a - Controller upgrade

Fixed problem of recently upgraded controllers
The 3 capacitors **C32**, **C33** and **C*x*** [replacing **C5**, **C28**, **C29** & **C30**] were inverse polarized.
On Controller #34, the fuse **F2** which had blown has been replaced.

### 2.1b - Controller testing

Already tested controllers: #9 & #49.
Tested 9 controllers: #1, #4, #5, #25, #33, #34, #43, #44 and #47.

[**AI #1**] Controllers #2, #38, #42 and #46 shall be repaired.

### 2.1c - Thermo-Electrical Cooler regulation

While the cooling and regulation of the chip temperature when Idle is satisfactory:

Cooling at max current (LED D15 is Red then Off),
Significant overshoot down to -34°C (LED D15 is Green),
Stable regulation at -30°C (LED D15 is Off),

Settling time approx. 300s

When acquiring images, the Peltier current drops to Zero during the readout time (300ms) and then shows a peak at `MAXIP` (3.2A) before re-entering the stable regulation regime.

Together with this effect, the temperature LED `D15` shows a short Green flash (CCD Too Cold indicator).

[**AI #2a**] This behavior should be understood and the PID component values tuned accordingly.

### 2.1d - ARC delivery

Most of the controllers delivered by ARC have shown following particularities:

- No factory default jumper setting
- The necessary settings are:
  - **B1** removed
  - **JP1** to **JP6** set
  - **JP9** set
  - **JP10** set
  - **JP11** set
  - **JP12** removed
  - **JP14** set
  - **JP15** removed
  - **JP16** removed
  - **SW2** set to position 3-1
  - **SW3** set to position 3-2
  - **SW4** set to position 3-2
- Chip temperature set-point
  The potentiometer **RW1** shall be adjusted to 0.52V for a temperature of -30°C.
- Alarm set points
  **R111** (Test pad **S1**) set to 3.4V (+20°C) driving the bit **CCD_HOT**
  **R113** (Test pad **S2**) set to 0.9V (-20°C) driving the bit **CCD_COLD**
  **R59** set to 0.9V (Peltier Max Voltage = 3.6V)
  **R61** set to 1.3V (Peltier Max Current = 3.6A)

[**AI #2b**] The factory configuration of the new controllers shall be part of the ordering.

## *2.2 - Deliveries*

### 2.2a - PRIMA STS delivery

1 CCD57-10 thick head #21 and Controller #47 + PMC #16 have been successfully delivered to FDE.

Complete equipment has been temporarily sent to Arcetri (Florence, Italy) for APE/PYPS.

### 2.2b - X-Shooter delivery

1 CCD57-10 thick head #22 and Controller #9 + PMC #37 have been successfully delivered to HDE.
Complete equipment has been installed in the Assembly Hall and been successfully put in operation.

### 2.2c - UVES upgrade

3 CCD57-10 thin heads #11 (Spare) #16 & #17 have been successfully tested.
3 Controllers #1, #25 & #49 have been successfully tested.

All equipment including PMCs #8, #20 & #23, extension cables and fibers have been shipped on Friday 17 Nov to Paranal (expected delivery Sunday 26th in time).

## *2.3 - Clock patterns*

### 2.3a - Clock patterns for E2V47

The observed horizontal jitter occurring on CCD47-20 in windowing has been understood as being a timing problem in the Serial Skip clock pattern. A delay of 1 (= 40ns) has been introduced that fixed the problem. Tests were done for any window size located anywhere on the chip up to the most distant border wrt. the output location.
The other delays for IS and S Parallel have been adjusted to 32.

### 2.3b - Clock patterns for E2V57

In the 2 window readout mode, some strange features (horizontal shift to the right of the first line, first and last common lines). A delay of 1 (= 40ns) has been introduced that fixed the problem.

### 2.3c - New clock patterns

For each chip 3 clock patterns have been developed:

- **`Usr`** : Image area only[512V × 512H] resp. [1024V × 1024H]
- **`Eng`** : Whole area [528V × 562H] resp. [1032V × 1074H]
  this pattern includes the prescans and overscans.
- **`Lab`** : Whole area [532V × 564H] resp. [1034V × 1076H]
  this pattern shows in **`_LR`** mode a 2 pixel gap in the middle of the image.

### 2.3d - Binning

The binning is now supported for E2V47.
Only binning factors 1, 2 or 4 are supported for both horizontal and vertical binning in any combination.
The problem related to the horizontal binning by 4 has been fixed.

When comparing the binned images obtained from the left and from the right output, one can observe an horizontal shift of 1 (binned) pixel. In two output mode, the 2 central columns do disappear. This is due to the way the readout pipeline is implemented as it first reads the pixel before clocking it. Therefore the first pixel left is not binned and is actually the last of the prescan region while the last binned pixel to be read is discarded as it is handled by a skip clock.

[**AI #3**] The solution would be to handle separately the first and the last pixels of the image.

### 2.3e - Retrofitting to JAN2006

The improvements of the clock patterns have been retrofitted to the driver **`arcdrv`** in version **2.1.2.1** for backwards compatibility with **`JAN2006`**.

### 2.3f - Binning and Windowing

[**AI #4**] This feature is not supported yet. It shall be implemented in the coming months.

### 2.3g - Windowing

Up to 2 windows (not overlapping) can be defined anywhere in the chip.
In two output mode, only one window shall be defined that is located in one half of the chip. It generates a second mirrored window.

### 2.3h - Bias Offsets

The Bias Offsets temporarily controlled by the global variables **`ccdrdbSBO_L`** and **`ccdrdbSBO_R`** for resp. the Left and the Right outputs. Their value is set by the boot script **`ccd.boot`**.
It is recommended to customize these setting in the application **`userScript`** with values that fit better.

[**AI #5**] A proper mechanism shall be implemented. This is actual part of the telemetry and should be driven by the configuration files **`ccdTecE2V*.dbcfg`**.

## *2.4 - Software*

### 2.4a - Temperature monitoring

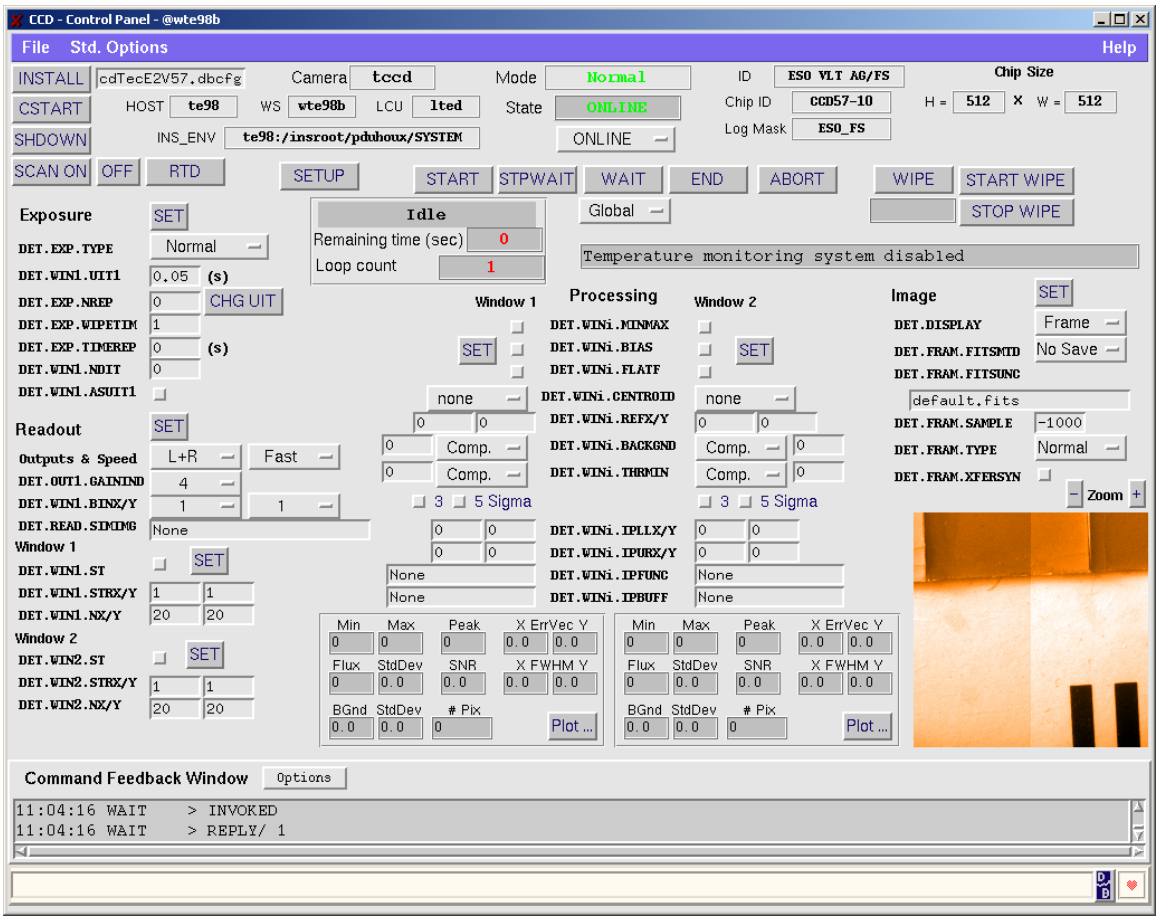
The temperature monitor has been implemented. It is checking once per minute or after each exposure the status of the Thermo-Electrical Cooler (Peltier).
If the status is not OK for more than 5 minutes, the CCD software state is deprecated to **`STANDBY`**. The Peltier cooler is consequently switched off.

### 2.4b - State machine

A transition problem has been detected and fixed with **`ccdcon 4.9`**.
The faulty transition was **`LOADED-Initialized`** → **`LOADED-NotInit`**
(Command **`OFF`** following a command **`INIT`**).

## 2.4c - New panel `ccdCtrlNB`

A dedicated panel has been developed for running on a LapTop (1024×788). It implements all the setup `FITS` keywords and includes a small `RTD` panel.




## 2.4d - Interrupts

The interrupts can now be fully configured by software. They are temporarily controlled by the global variable **`ccdrdbEPI`** which takes the values 0 to 3:

0: No Interrupt
1: Command Completion Interrupt
2: Image Transfer Completion Interrupt (`DMA`)
3: Both interrupts

This setting takes effect with the **`INIT`** command.

| | |
|---|---|
| On the CPU board Actis | `VSBC6847`, this value shall be set to 2. |
| On the CPU board Motorola | `MVME2604` |
| & | `MVME2700`, this value shall be set to 2. |
| On the CPU board Motorola | `MVME6100`, this value shall be set to 2. |

[**AI #6**] A proper interrupt configuration mechanism shall be implemented.

### 2.4e - Configuration files

Associated to the clock patterns, the two CCD chips CCD57-10 and CCD47-20 can be configured (via shell command **`ccdInstall.sh`**) using the files:

- **`ccdTecE2V57.dbcfg`** which associates the clock file **`acetecE2V57.clk`** and operates in **`USR`** mode [512H × 512V].
- **`ccdTecE2V57_ENG.dbcfg`** which associates the clock file **`acetecE2V57_ENG.clk`** and operates in **`ENG`** mode [562H × 528V].
- **`ccdTecE2V57_LAB.dbcfg`** which associates the clock file **`acetecE2V57_LAB.clk`** and operates in **`LAB`** mode [564H × 532V].

and

- **`ccdTecE2V47.dbcfg`** which associates the clock file **`acetecE2V47.clk`** and operates in **`USR`** mode [1024H × 1024V].
- **`ccdTecE2V47_ENG.dbcfg`** which associates the clock file **`acetecE2V47_ENG.clk`** and operates in **`ENG`** mode [1074H × 1032V].
- **`ccdTecE2V47_LAB.dbcfg`** which associates the clock file **`acetecE2V47_LAB.clk`** and operates in **`LAB`** mode [1076H × 1032V].

Both **`ENG`** and **`LAB`** modes include prescan and overscan rows and columns.

### 2.4f - CCD Software FEB2007

The CCD Software bases on the upgraded BSPs for PCI support. These BSPs are archived in the module **`vltVXWORKS`** version **`3.17.2.2`** (**`3.18`**).

The public interface to the CCD Software is unchanged wrt. **`JAN2006`**.
Only the 2 modules specific to the control of the new controller have been upgraded.

The build module is **`ccdint`** version **`7.17`**.

# 3 - Pending Issues

## *3.1 – Actions Items*

[**AI #1**] Controllers #2, #38, #42 and #46 shall be repaired.
[**AI #2a**] The TEC behavior should be understood and the PID component values tuned accordingly.
[**AI #2b**] The factory configuration of the new controllers shall be part of the ordering.
[**AI #3**] The readout sequence for binning should be improved: a solution would be to handle separately the first and the last pixels of the image.
[**AI #4**] The windowed readout with binning feature is not supported yet. It shall be implemented in the coming months.
[**AI #5**] A proper telemetry configuration mechanism shall be implemented.
This is actual part of the telemetry and should be driven by the configuration files **`ccdTecE2V*.dbcfg`**.
[**AI #6**] A proper interrupt configuration mechanism shall be implemented.

## *3.2 – PCI Interface*

The detailed PCI bus configuration shall be refined for each platform in order to improve the robustness of the system.

## *3.3 – Software*

In polling mode, the Image Transfer completion condition is detected too early wrt. the effective data transfer.
It seems that the Actis board VSBC6847 is hanging in Polling mode during readout. This may be due to the PCI bus configuration.

**___oOo___**