ALMA
SIS Process Development to serve Next Generation Receivers for ALMA
Final Study Review report

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Change Record

Version	Date	Affected Section(s)	Change Request #	Reason/Initiation/Remarks
A	2024-03-15	All		New document.
B	2024-05-20	All		Updates in response to the Final review panel report [1]. Appendix I contains tracking of the addressed Ais.
C	2024-07-01	All		Final cleaned-up version

Contents

Introduction

The study **"SIS junctions process development to serve Next Generation Receivers for ALMA"** [2] follows the ALMA Development Roadmap [3], which sets the "*long-term development strategy, where the priorities in the coming decade are an increase of the receiver* ***IF bandwidth by at least a factor of two***" to address the three new fundamental science drivers: the origin of galaxies, the origins of chemical complexity and the origin of planets.

From the SIS mixer device prospective, the goal of increasing the IF bandwidth by at least a factor of two translates into requirement to decrease of and keep tight control over the SIS junction capacitance, which is responsible for IF response roll off at higher frequencies. In turn, that calls for (1) the SIS junctions with a smaller area and, hence, capacitance, and (2) SIS junctions tunnel barrier having a lower specific capacitance, Nb/Al-AlN/Nb, should further be carefully characterized in respect to its specific capacitance.

The content of this Final Study Review report follows the items as defined by the Statement of Work, Delivery ID# DS2 [2]:

1. Technical report, including:
    a. final selection and description of fabrication process for small size SIS junctions and custom-shape SIS chips, in case the last found necessary.
    b. fabrication and dc characterization of small size SIS junctions, measured geometries, parameters, quality, yield.
2. Fabrication and delivery to NOVA Band 9 SIS mixer demonstrator according to their design.
3. Technical report by NOVA, including:
    a. dc and heterodyne characterization of the Band 9 SIS mixer demonstrator.
    b. analysis of performances of the Band 9 SIS mixer demonstrator and comparison with simulations.

1 SIS junction process development

1.1 Final selection of fabrication process for small size SIS junctions

In the scope of the study, the three alternative lithography techniques for defining the SIS junction pattern have been considered: direct laser writing, e-beam lithography, and stepper lithography. Among the three alternatives, we have considered the following selection criteria summarized in the Table 1 and as a result, we have identified and made the choice of the lithography method for defining the SIS junction area.

Direct laser writing (DLW) is the most attractive technique to attempt employing, because:

- That is readily available in the pool of equipment of Chalmers nanofabricating facility. It is well supported and has recently been expanded by purchasing yet another new machine[1].
- Employing direct laser writing for SIS junction pattern definition does not call for any significant change in the overall processing flow. This allowed for quick process development. It was not clear from the beginning whether DLW technique allows achieving the targeted ≤1 μm^2 size of SIS junction. However, we have succeeded to develop the process and demonstrated feasibility of patterning of SIS junctions with small enough area (see the Sections 1.2.1 and 1.2.2 for the more details).

Electron-beam lithography (EBL) certainly allows to achieve the junction size goal. Also, it is readily available in the Chalmers nanofabricating facility. However, in contrast to DLW, moving to the EBL calls for quite extensive re-establishing of the overall processing flow for SIS junctions, as the electron resists are very different in their technological properties. Not least, the EBL systems in the lab are quite heavily booked and characterized by about twice more expensive machine hours together with quite long machine time needed. Because of these factors, we considered this alternative only as backup, if it were not possible to achieve the targeted junction area with DWL. However, as it is shown in the Paragraph 1.2.1, we have achieved the goal with the DWL, and hence, we did not explore the EBL alternative further.

Finally, **stepper lithography** could be highly attractive, as it combines necessary size definition capabilities, excellent automated overlay alignment accuracy and quick writing speed. Also, it is probably less than EBL calling for re-establishing of overall processing flow. The stepper lithography, however, is very restrictive towards the substrates, which are compatible with stepper processing. Those are only big size round wafers (certainly, not less than 4" diameter), which are compatible. This puts both additional technological and budget pressure in case the stepper lithography is employed. The big round wafers of z-cut quartz are quite expensive and not so easily available. Also, the big wafers are always significantly thicker (typically, thicker than 0.5mm) than practical SIS mixer designs require. Ultimate requirements stepper lithography puts for the wafer flatness and parallelism are almost prohibitive for considering thinner wafer mounting over the thick carrier wafer. Altogether, lapping, or deep etching of wafers become just a compulsory last step in the SIS junction process flow. This is a significant complication and additional risk factor from the overall processing perspective. Last but not at all the least, stepper lithography is not available in-house, but only through µFab network cooperation, in the Stockholm area. All-in-all, the stepper lithography option was to be considered as a last resort, only in the case of DWL and EBL both failed to ensure required outcome. That turned out not to be the case, and hence, this alternative was not explored further in this study.

[1] Heidelberg Instruments' DWL-2000 was used for the processing in the current study. Yet another Heidelberg's MLA-150 has recently been to the pool of the equipment.

Table 1 Selection criteria for microlithography technique for fabrication of the small junctions

Technique	**Junction size definition** **Requirement:** • **Capable of defining ≤1μm²**	**Effort for fabrication process integration** **Requirement:** • **Affordable within the allocated study**	**Availability / machine time cost** **Requirement:** • **Readily available** • **Affordable within the allocated study and beyond**	**Requirement to the substrate material** **Requirement:** • **Flexibility in respect to the substrate lateral size and thickness**
Direct laser writing	✓ *Proved to be ok*	✓ *Least* the overall process is standard!	✓ *Readily available* in-house at the modest hour cost	✓ *Virtually any substrate* The only important requirement is substrate's flatness[2]
E-beam lithography	✓ *with a significant margin*	– *High* e-beam resists are very different to UV ones in thickness, baking temperature, plasma stability, lift-off and stripping properties	± Available in-house, but *heavily booked*. About four times higher hour cost of DWL! About triple slower than DWL	✓ *virtually any substrate*
Stepper lithography	✓ ok	– *High* Likely calls for backside lapping and/or especial substrate mounting to be developed	– *Not available in-house*, access through MyFab network in Stockholm area. More than triple hour cost of DWL	– Only round wafers, min. 4" diameter and quite thick (ca. 500μm), prohibitively expensive, if crystal quartz needed

To summarize, Direct Laser Writing is the lithography process of the choice for the purpose of defining the SIS junction area. It allowed minimal changes to the very stable standard SIS process, is readily available in-house, has a modest hour cost of the machine time and quick writing speed. Use of Electron Beam Lithography is not seen justified for the purpose based on significantly stronger modification of the fabricating flow required. Additionally, EBL is heavily used, has a four-fold machine-hour cost and slower writing speed. The EBL alternative could be explored in future, if motivated by the requirements from the SIS device design side not satisfied by the capabilities of the DWL technology.

1.2 Description of fabrication process for small size SIS junctions

The fabrication process is based on the standard GARD SIS process [4], which is well established and was used for virtually all SIS devices for the mixer receivers developed and produced by GARD, e.g. ALMA Band 5 [5]–[7], APEX SHeFI [8]–[11] and Sepia [12], [13] instruments. The standard process had

[2] Regular micro lithography grade substrates (local or site TIR (total indicated reading within ca. 1.5 μm, site size ca. 10x10 mm) are very well suitable. The (very) local pits defects, like those sometimes found, e.g., on the z-cut crystal quartz substrates, cannot be acceptable due to the specifics of the pneumatic height sensing for the beam focusing, which integrates the height information at the area of ca. 3mm around the focusing point.

been complimented with the option of AlN tunnel barrier layer [14], [15] in course of the preceding ESO study [16], [17] and further upgraded within this study with the process for ≤1 μm^2 junction area definition.

The baseline SIS process at GARD consists of five topology layers.

First, the Nb tunnel structure, also often named as "*trilayer*", is grown over the whole area of a wafer and includes three metal layers and tunnel barrier layer: bottom Nb layer (typically, 200nm thick), Al layer (ca. 7 nm thick), tunnel layer of AlO_x (thermally oxidized) or AlN (plasma nitridized), and top Nb layer (typically, 100 nm thick). The supported tunnel barrier resistivity, R_nA product (where Rn is SIS junction's normal resistance, and A is junction's area), is down to 20 Ω·μm^2 for AlO_x barrier layer SIS junctions, and down to 5 Ω·μm^2 for AlN barrier layer SIS junctions. The first topology layer is then patterned with the first superconducting metallization layer shape. This topology layer is further referred as *BASE* layer.

Second, the pattern of SIS junction and interlayer insulation around that is shaped (further referred as *IJ1* layer). That is where the focus of this study is placed. As presented above in the Paragraph 1.1, for the purpose of defining the SIS junction patterns, Direct Laser Writing was selected. The details of the lithography process are summarized below in the Paragraph 1.2.1. Further, the SiO_2 dielectric layer is sputtered and lifted-off. The supported thickness of this (first) SiO_2 layer is within 100…300 nm range.

Third, the second dielectric layer can be deposited and patterned by lift-off. This is the optional layer, which often but not necessarily is used by the SIS mixer layout. The supported thickness of this (second) SiO_2 layer is within 100…300 nm range. This topology layer is referred as *IJ2* layer.

Fourth, the second superconducting metallization layer, Nb, is grown and further patterned after. The supported thickness of this Nb layer is up to 350 nm. This topology layer is further referred as *COUNTER* layer.

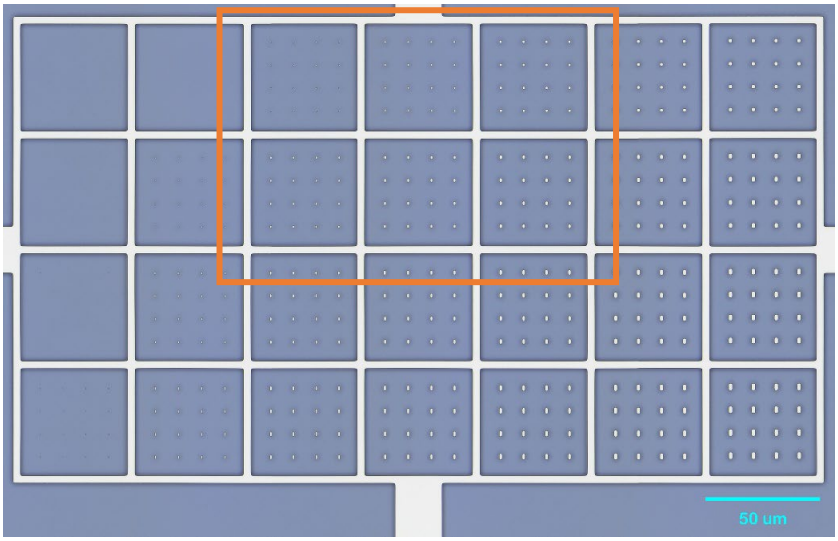
Finally, the contact pads to interface the circuitry external to SIS junction chip or wafer are fabricated. The supported system for the contact metallization is Nb (50…100nm)/Pd (100…200 nm). This topology layer is further referred as PADs layer.

1.2.1 Pattern definition for the small SIS junctions.

The direct laser writer available in-house has a particular UV wavelength, 405nm. There is a modest selection of alternatives of the suitable photo resists to consider for this UV wavelength. The identified product AR-N 4340 from Allresist GmbH had been evaluated, and further implemented as the baseline resist for SIS junction process at GARD [18].

The test patterns ranging from nominally 0.4 × 0.4 to 1.6 × 3 μm^2 have been used for the process optimization. The results of the DWL exposure optimization have been followed by reactive ion etching process of 100 nm Nb layer through the created resist stencils and consequent deposition and lift-off of 200 nm SiO_2 layer (Figure 1) demonstrated feasibility of definition of submicron patterns for SIS junctions. That presents the standard process sequence used for SIS junction definition and hence, proves the developed small junction definition approach is not only lithographically feasible, but also compatible with the rest of the SIS junction processing.

a)



b)

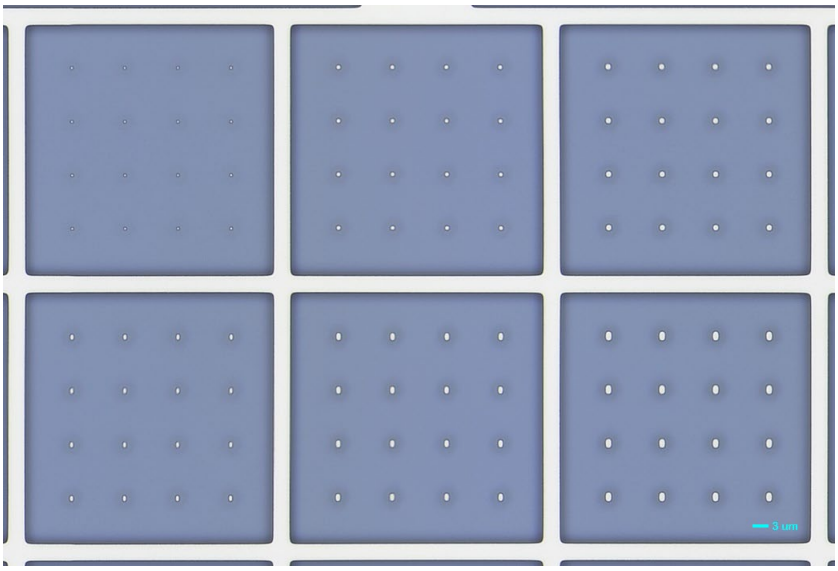


Figure 1. (a) Optical micrograph of test pattern in Nb layer defined by the resist AR-N 4340 from Allresist GmbH, stencils nominal area range ca. 0.2…5 μm^2. (b) Expanded view of the part of the image framed in orange at the photo (a).

After setting up the DWL exposure process for the AR-N 4340 resist, the small SIS junction definition process was integrated with the rest of the GARD standard SIS process. Figure 2 presents an example of scanning electron microscopy images demonstrating a 1 μm^2 junction pattern.

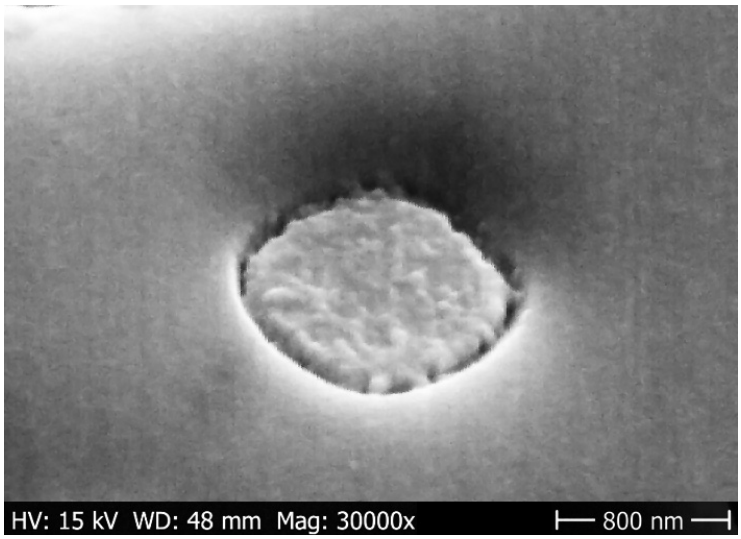


Figure 2. SEM image of a defined SIS junction pattern of ca. 1.15 μm diameter (1 μm² area)

1.2.2 Fabrication and dc characterization of small size SIS junctions

A number of batches of the test junctions were fabricated. All fabricated junctions demonstrated excellent quality, e.g. Figure 3. Also, measured at the wafer level, the fabricated batches always demonstrated yield well above 80%, meaning by that the healthy SIS junction. From the perspective of the yield of the SIS devices for usage in the practical mixers, that also has been proven to be as high as 80%[3] (more details are communicated in the Paragraph 3.1).

Extracting the junctions' dimensions through analysis of microscopy images is a tedious process, but also the results are not very accurate because the image of the SIS is influenced by the deposited thick Nb layer of the second superconducting metallization. For this reason, for extracting the junctions' area, we used the following approach. Each wafer had a set of bigger sized test junctions of the round shape. Assuming round junctions' dimensions experience uniform offset due to the fabrication process, it is possible to extract the true SIS junctions' resistivity, R_nA, from the dependence of junction's normal resistance on the junction's area (Figure 5). Further, assuming the junctions' resistivity, R_nA, is constant over the wafer, it is possible to use measured normal resistance of junction as the measure of its area and extract it as a ratio of R/R_nA.

Applying this approach, the example of the true junctions' areas estimated from the SIS normal resistance and the extracted R_nA is demonstrated in the Table 2. The junction area values in the Table 2 are derived assuming the R_nA product of 8.4 Ohm μm² as follows from the Figure 5. The data corresponding to the bigger round shaped test junctions is colored in pink. The test junctions of different areas and shape could be fabricated. It has also been demonstrated that quite small junctions could be fabricated, down to 0.2 μm². R_j/R_n ratio measured at the 0.2 μm² junction is somewhat lower (Figure 3 c,d), but it could, as follows from the discussion below, be also the measurement limited.

The measurement of SIS junctions' current-voltage characteristics reported here and further all were performed by sweeping current from maximal (positive) down through zero and further to minimal (negative) bias current. This way, the curve in the positive quadrant presents normal resistive branch,

[3] The SIS junction yield 80% found by NOVA group after measurement at the chip level after lapping and dicing suggests junctions which are healthy, i.e. neither short, nor open. Those alive junctions usually all have high quality.

gap and subgap branches of the current-voltage characteristic. The curve in the negative quadrant presents Josephson superconducting current, followed, after reaching the SIS junction's superconducting critical current, by the part of the gap and normal resistive branches of the current-voltage characteristics.

The recorded current-voltage characteristics were further processed to account for current and voltage offsets present in the measurement system. For that, the negative quadrant of the current-voltage characteristic was mirrored in respect to the voltage and current axis and the origin of the plot was adjusted to reach the best fit of normal resistive and gap branches of the current-voltage characteristic. The critical current branch should also appear at exact zero voltage.

The R_j/R_n ratio is further extracted as the slope of the straight line driven through the plot origin and touching (tangential) from the below the SIS junction's current-voltage characteristic. The procedure may lead to underestimation of the junction's R_j/R_n ratio in case the current noise in the measurement system or resonances at the current-voltage characteristics cause jumping the state from the quasiparticle (subgap) branch to the Josephson superconducting current branch, as seen, e.g., at the Figure 3 d.

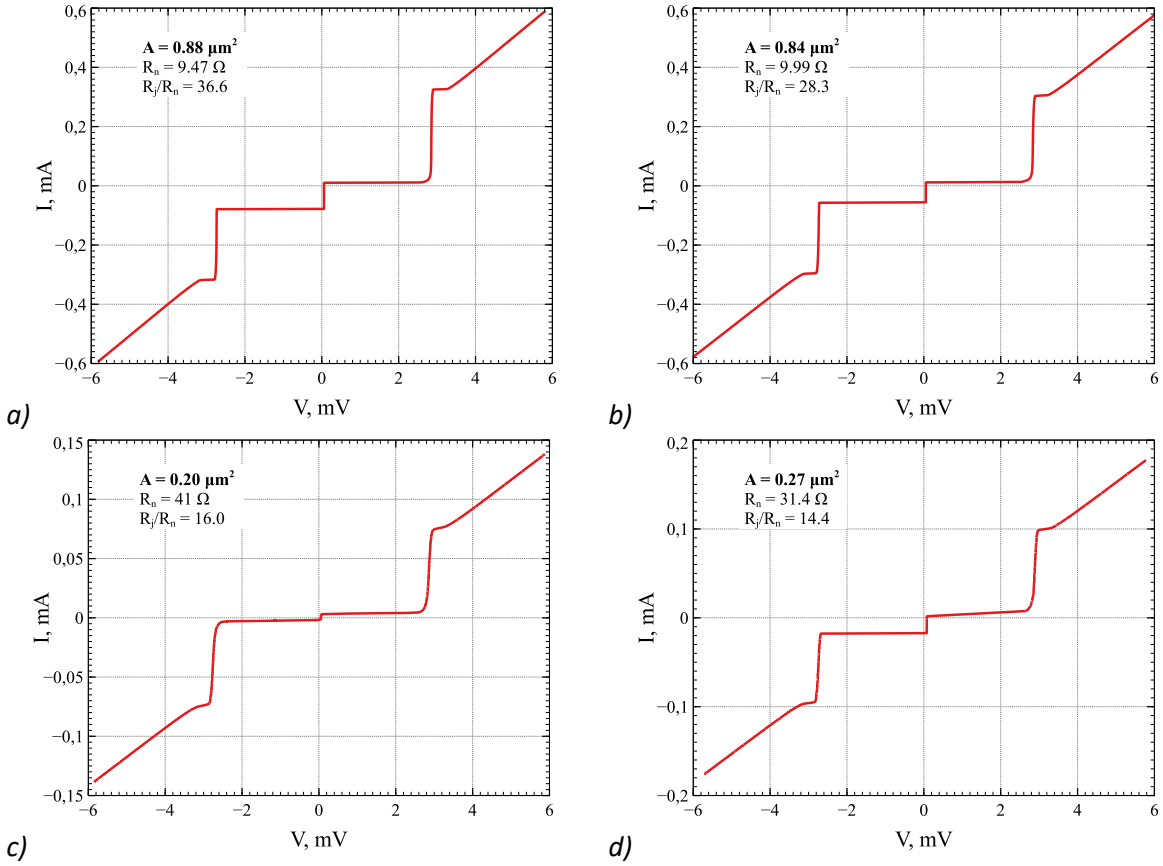


Figure 3. Current-voltage characteristics of Nb/Al-AlN/Nb SIS junctions with the RnA product of 8.4 Ohm·μm² with the area of ca. 0.85 μm² (a), (b), and those with the area of ca. 0.25 μm² (c), (d). The measurements were performed with a dipstick at 4.2 K liquid helium temperature at atmospheric pressure.

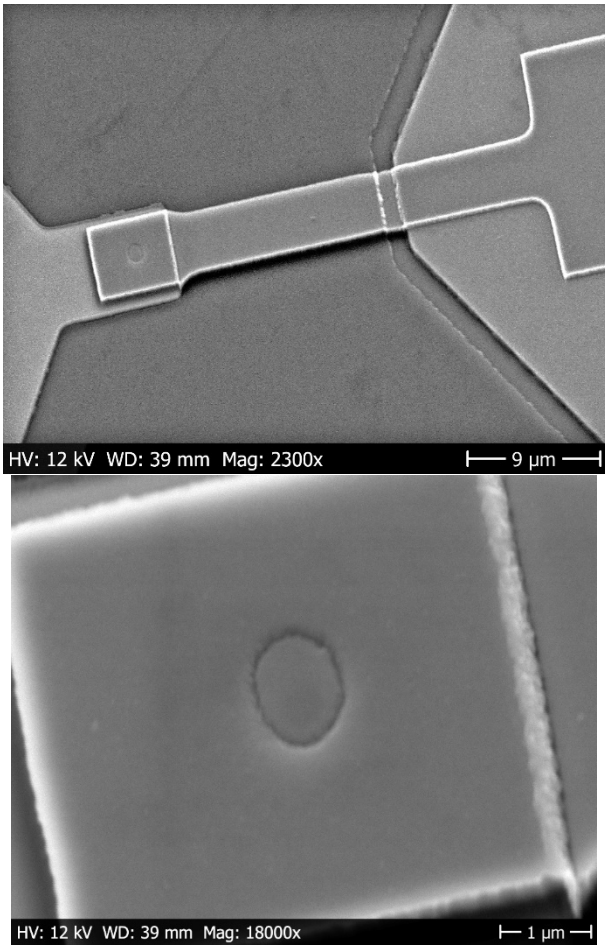


Figure 4. SEM image of a defined SIS junction taken at ca. 40° tilt.

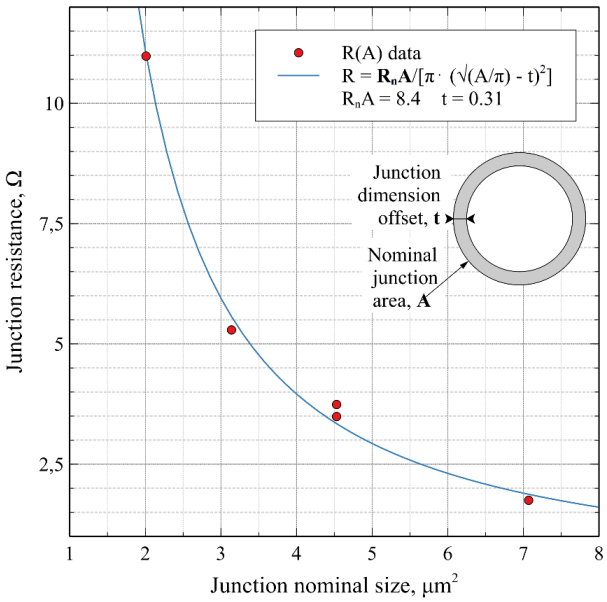


Figure 5 Extracting of the junctions' R_nA product.

Table 2 Measured normal resistance and the estimated true area of the junctions.

Rn, Ohm	A, μm², estimated[4]	Nominal shape and size, μm
1,75	4,80	Round, dia. 3.0
3,74	2,25	Round, dia. 2.4
3,49	2,41	Round, dia. 2.4
5,29	1,59	Round, dia. 2.0
10,98	0,77	Round, dia. 1.6
9,99	0,84	Rectangular, 0.8x2.4
9,47	0,88	Rectangular, 0.8x2.4
11,44	0,73	Rectangular, 1x2
15,24	0,55	Rectangular, 0.8x1.6
17,08	0,49	Rectangular, 0.8x1.6
22,40	0,38	Rectangular, 0.6x1.8
31,37	0,27	Rectangular, 0.6x1.8
31,31	0,27	Rectangular, 1x1
41,00	0,20	Rectangular, 0.6x1.2
51,91	0,16	Rectangular, 0.8x0.8

Illustrating the difference between junction area estimated from SIS junction image and from its normal resistance and wafer's R_nA, Figure 4 shows the oval shaped junction of ca. 1.6 × 0.8 μm² (i.e., 1 μm² area), but estimated through its normal resistance (in Table 2), turned out to be ca. 0.5 μm² area.

1.2.3 Specific capacitance of SIS junctions

The knowledge of SIS junction specific capacitance, C_s, is crucial for performing SIS mixer designs. For this reason, in the first part of this study, the comparison of the specific capacitance of GARD's SIS junctions characterized at GARD and NAOJ was performed and reported [18]. Figure 7 presents the summary of the C_s *vs* R_nA characterization of SIS junctions.

[4] The junction area values are estimated assuming the R_nA product of 8.4 Ohm μm² as follows from the Figure 5.

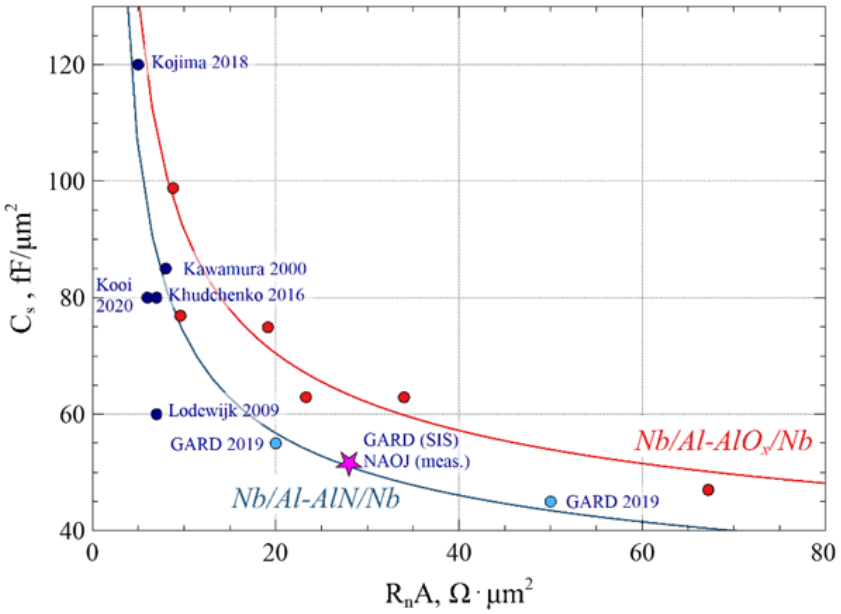


Figure 6. Comparison of the C_s numbers extracted at NAOJ with direct measurements in cryogenic probe station with those extracted earlier by GARD as well as by the other groups[5]. The magenta-colored star symbol with label "GARD (SIS)/NAOJ (meas.)" applies to the data measured at NAOJ on the AlN-barrier SIS junction sample device fabricated at GARD. The light blue dots label the data points, where the C_s data had been extracted by GARD cryogenic S-parameter measurements technique [19] *of the AlN-barrier SIS junctions. Dark blue dots show the data extracted by other groups. For comparison, the extracted at GARD data for AlOx-barrier SIS junctions is shown with the red dots* [20]*. The capacitance data for the junctions are approximated with semi-empirical relation $C_s = a / \ln(R_n A)$,* [21]*, where a is equal to 211* [20] *for the Nb/Al-AlO$_x$/Nb junctions and to 170 for the measured Nb/Al-AlN/Nb junctions.*

1.2.4 Further process development activities

In the spirit of the readiness for SIS devices fabrication for ALMA Next Generation receivers, attention also was paid to improving repeatability of SIS junction's resistivity R_nA between the fabrication batches.

It was earlier well recognized that the **vacuum conditions** in the nitridation chamber play an important role in reproducibility of junctions' R_nA.

- The sputtering system configuration is such that plasma nitridation process coexists in the same processing chamber with deposition of silicon oxide. Silicon oxide deposition is vital for SIS junctions processing and cannot be isolated to another deposition chamber. The deposition of silicon oxide contributes to the chamber walls saturation with absorbed oxygen, which later can contribute to forming of the SIS tunnel barrier. Addressing this concern, the chamber conditioning stage was introduced to standardize the vacuum conditions. This includes multiple rinsing of the nitridation chamber with nitrogen and argon.
- Vacuum recovery after chamber venting, either those due to planned maintenance or caused by e.g. blackouts. Both are quite seldom. Still, long pumping followed by the sequence of chamber rinsing with dry nitrogen and/or argon are both essential.
- It was recognized that the nitrogen plasma source itself presents a sort of a trap for absorbed oxygen and humidity from the room air. To address this problem, the plasma source

[5] Kawamura 2000 [25], Khudchenko 2016 [26], Kojima 2018 [27], Kooi 2020 [28], Lodewijk 2009 [29]

conditioning step has been introduced prior to the barrier nitridation as a part of chamber conditioning, together with argon and nitrogen chamber rinsing.

The **plasma condition** at the substrate is also an important factor of repeatability of the junctions' R_nA. With this understanding, the substrate was always placed outside the active plasma region. The electron current sinking to the substrate was always being monitored during the nitridation process. Later, it was noticed that the resistance for electron current to the ground could be different due to different factors. To check whether that is the significant factor, we have fabricated two batches of the samples, quite identical otherwise, but one had the substrate floating and another shorted to the ground with as low resistance as was possible. The results are presented at the plots on the Figure 7. That is vividly seen that the resulting R_nA is three times lower when the substrate is short circuited to ground during the barrier nitridation. Additionally, the junction quality was noticeably better for nitridation on the grounded substrate. Altogether, that leads to the decision to short-circuit the substrate to ground for better R_nA repeatability.

1.2.5 Regarding custom shaping of SIS mixer chips

This project activity is envisaged to be performed in case design effort within the another study (ALMA Band 6 and 7 demonstrator [22]) will demand such technology.

In the frame of this activity, we committed to supply another ESO study, Band 6 and 7 demonstrator [22], with the SIS device chips. The status of this study [22]–[24] proves that yet with the traditional rectangular chip shape, the RF and IF bandwidth goals could be achieved. Hence, development of the custom SIS mixer chip shaping was not motivated.

2 Fabrication and delivery to NOVA Band 9 SIS mixer demonstrator according to their design

In the frame of this study, we have fabricated a batch of Band 9 demonstrator mixer chips following the process developed in this study. The batch was fabricated on the fused quartz substrates delivered by NOVA. The SIS junction area was designed to be 1 μm^2 and 0.7 μm^2. The overall fabrication process was successful.

The wafer was delivered to NOVA in October 2023.

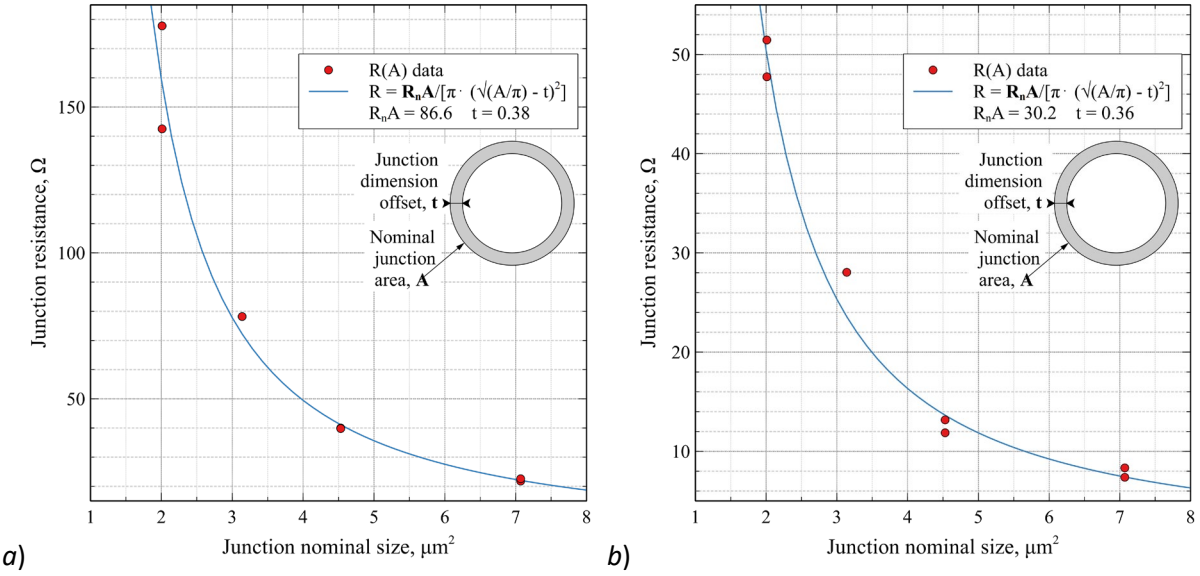


Figure 7 Extracted R_nA values for the two batches of Nb/Al-AlN/Nb SIS junction fabricated with the substrate at the floating potential (a) and short circuited to ground (b) during plasma nitridation of the tunnel barriers.

The DC characterization of the fabricated junctions has been performed on the wafer level at GARD and later complimented by that at the chip level upon their lapping and dicing at NOVA (Figure 8). The R_nA of the junctions in the batch was about 13 Ω·μm². Assuming R_nA uniform across the wafer, the junctions' R_n can be understood as the measure of their areas. This way, the area of the junctions at the chips tested at NOVA have been shown to be ca. 1.1 and 0.8 μm², i.e. close to that designed and defined by the Direct Laser Writing. From the Figure 8, one can see that the test junctions measured at the wafer level are a bit smaller (having a bit bigger dimensional offset) than those measured on the single chips after the wafer dicing. That is due to the test junctions are the closest to the wafer edges, while the mixer chips belong to the interior area of the wafer. That is known and usual fabrication process effect common for all batches of any junctions fabricated by GARD process. Also, the observed higher scattering of normal resistance of the junctions of bigger nominal area (Figure 8) reflects the fact that the substrate had flatness defect at the place where the most of "outliers" of bigger size were located.

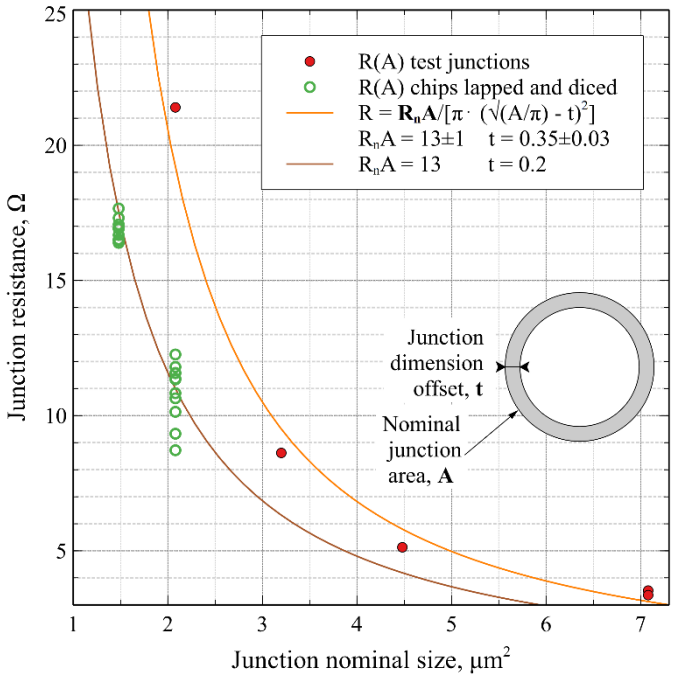


Figure 8 The extracted R_nA number for the batch of Nb/Al-AlN/Nb SIS junctions for Band 9.

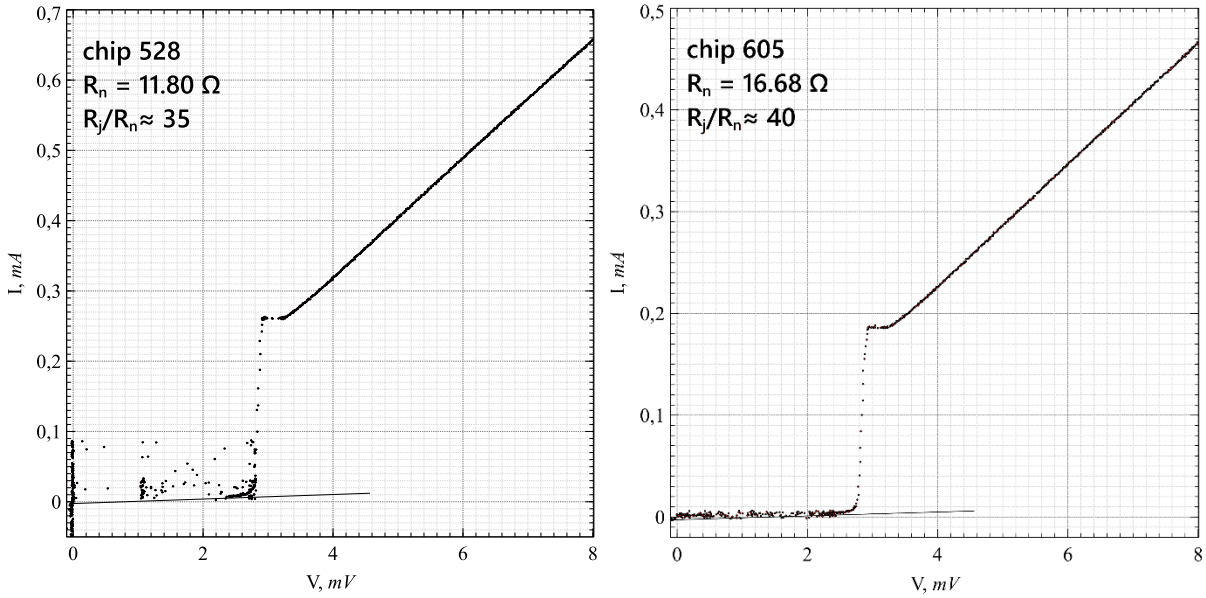


Figure 9 Current-voltage characteristics of the junctions from the chips 528 and 605 used in the RF characterization of the Band 9 demonstrator mixers (further described in the Paragraph 3.1).

Measurements at the chip level done at NOVA support recording of the SIS junction IVC with carefully suppressed Josephson current. This allowed accurate recording of the subgap part of the junction IVC and hence, assessment of the junctions' quality characterized by the R_j/R_n ratio. Figure 9 presents the IVCs of the junctions used in the RF characterization of the Band 9 demonstrator mixers (further described in the Paragraph 3.1). Both devices demonstrate the junctions with very high quality, $R_j/R_n \geq 35$.

3 Band 9 SIS mixer demonstrator [6]

3.1 DC and heterodyne characterization of the Band 9 SIS mixer demonstrator

3.1.1 Mask design implementation

The original ALMA band 9 design has been recalculated using CST Microwave studio package to adapt for Chalmers University design rules. Main modification was the increase of SIS junction size from 0.5 μm^2 to a 1 μm^2. Parameters of impedance transformer and inductor have been changed accordingly to achieve appropriate band coverage. Figure 10, in its upper part, shows the implementation mask layout. It contains three sectors with 86 mixer positions each totaling 258 junctions. Several positions contain junctions of different areas connected to large DC pads to evaluate the dc characteristics without dicing the substrate. On the lower panel of Figure 10, we present mixer structures as implemented. Apart from an increased junction's size, choke filters are also implemented in ground plane layer (red on the picture) while tuning structure is all in the wiring layer (blue in the picture). A large area through contact from wiring to the ground layers is implemented, which is new compared with original ALMA band 9 design. This modification has been evaluated to have no significant impact on the performance (both RF and IF).

Each of the three sectors have identical layout design except for junction areas. There are two groups of design implemented with junction areas nominally 1 and 0.7 μm^2.

3.1.2 DC tests

A test mask set was manufactured in Chalmers and the pilot batch of the SIS mixer junctions has been received. At the same time, RUG/NOVA group purchased a dicing machine, which was successfully installed. Using the receiver batch RUG successfully recovered the polishing and dicing. The first DC testing was a success. A high quality I-V curves were measured with an example shown in Figure 11. The quality of I-V curve is sufficient for heterodyne tests. The quality factor measured as Idc(2mv)/Idc(3mv) as high as 30, based on I-V characteristics with an applied magnetic field. It should be noted that this Q-factor is significantly higher than the one measured for nominal ALMA band 9 SIS junctions used in the receivers that are installed at ALMA. The average Q-factor of measured new batch junctions is 30 and the maximum value is 42 while minimum is 20. For ALMA band 9 junctions the Q-factor was in the range of 10…20. The knee structure is visible just above the I-V curve gap (3mv) region. This structure is due to proximity effect in the SIS junction layers around the tunnel barrier. Due to the large size of photon assisted tunneling step at 650 GHz band this knee structure has been found to have no significant effect to the heterodyne performance and stability.

[6] Contributed by A. Baryshev, S. Realini, R. Hesper, Rob de Haan Tijkel, M. Bekema, Jan Barkhof, Kirill Rudakov (all – at NOVA)

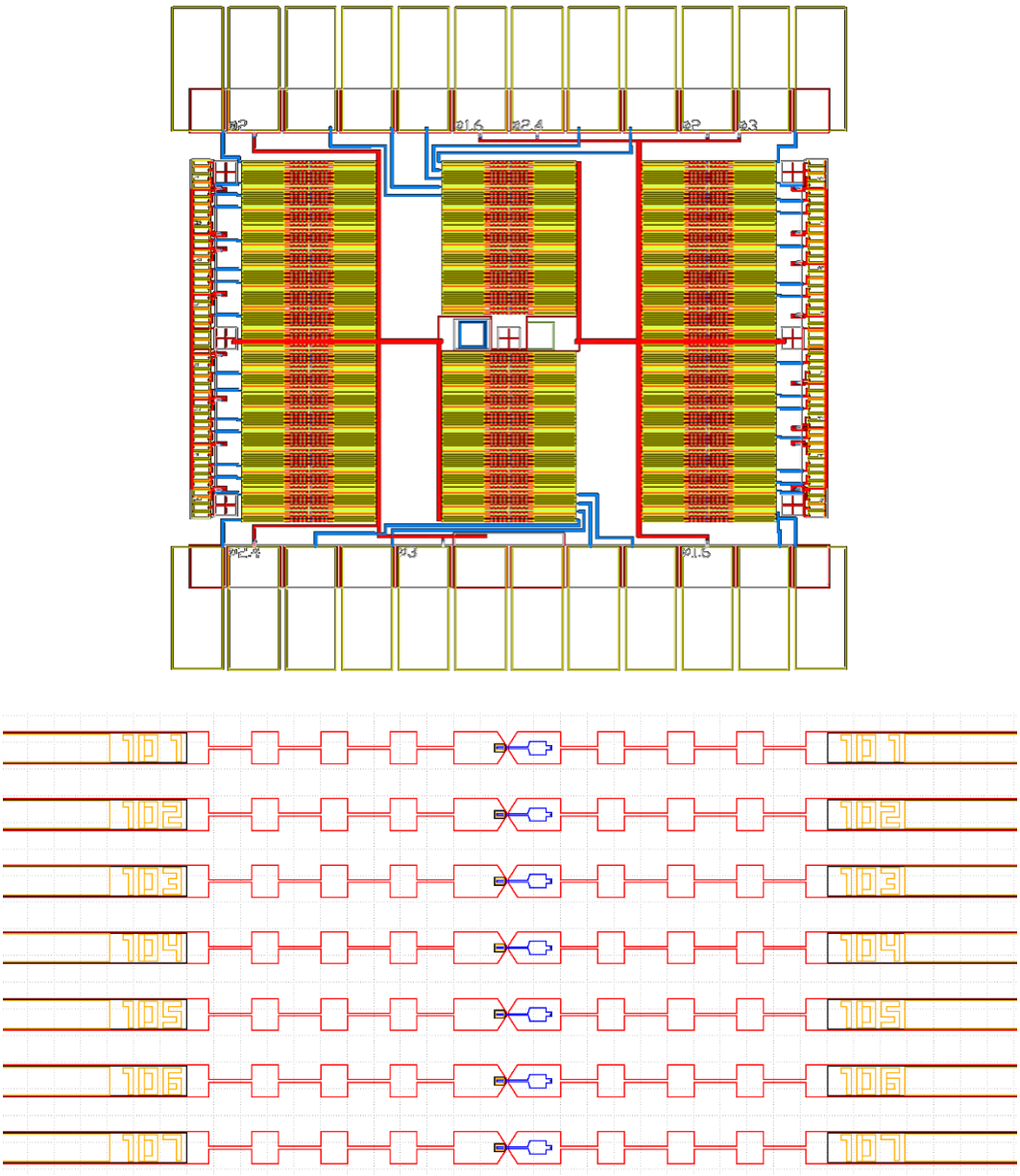


Figure 10. Layout of test batch depicting 3 sectors and DC test contacts (above), and layout of mixer structures (below) showing rows of mixer structures.

The normal resistance of nominal junction's size groups was found ca. 11 and 16 Ohms. With an RnA value of 13 determined earlier the junction's areas were 1.1 and 0.8 μm^2

Table 3 summarizes the dicing yield and dipstick yield achieved during processing. Note that only part of junctions has been DC tested yet. Based on this result, the total yield is higher than that we had during production of ALMA band 9. While it is still a low-number statistics, we can estimate the DC junction yield as 80$\pm$20%. This dc yield is in line with our experience during ALMA band 9 production project. According to these statistics, we already should have ~68 junctions of one design with good I-V from this batch.

Table 3, summarizing DC/Dicing YIELD

sector	*junctions*	*diced*	*polished*	*lost*	*dipstick results*

	from	*to*		*from*	*to*		*ok*	*fail*	*% ok*
1	101	143	all						
1	201	243	all						
2	501	537	all	516	530	0	12	3	80
2	601	641	all	601	615	1	11	3	78
3	301	343	all						
3	401	443	all						

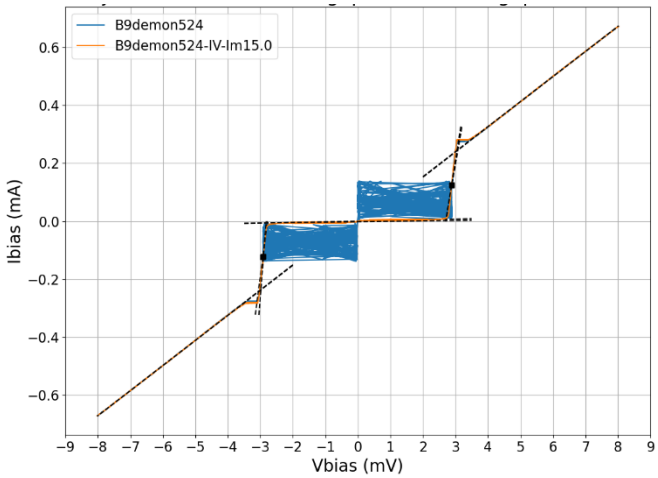


Figure 11. Measured I-V curve of one of the junctions showing nominal gap voltage and high quality factor >30.

3.2 Heterodyne cryostat tests

3.2.1 Heterodyne tests

In our heterodyne test program, we have further evaluated four mixers utilizing junction numbers 528 (Rn=11Ohm),606, 605, 608 (Rn=16 Ohm). We first tested junction 528 and 606 in order to select the best performing junction's area design and then tested 605 and 608 to gain an insight into reliability or RF yield. Heterodyne tests were performed in ALMA band 9 test cartridge which had identical configuration with ALMA band 9 DSB receivers which are installed in ALMA. Furthermore, the same set up and same test procedure has been used to measure the performance of SIS mixers. The cryostat cold stage was maintained at 4K, like for all ALMA performance tests. The IF configuration is the same as it is used in ALMA band 9, i.e. we use cryogenic isolator in 4-12 GHz band to match the SIS mixer and the IF amplifier.

We have further evaluated two mixer chips: junction 528 (Rn = 11.8 Ohms) on pol 0 and junction 605 (Rn = 16.6 Ohms) on pol 1. We evaluated receiver noise in a standard ALMA band 9 DSB test set as a part of ALMA band 9 DSB cartridge receiver. Figure 12 shows the achieved total IF band noise performance of the mixers. The mixer from pol 1 show an optimum performance. Actually, it is an improvement with respect to typical Delft technology mixers. The optimal response of pol 0 is shifted lower, as it is expected for a junction with ~1.4 times larger area. We also note a smooth magnetic field Josephson noise suppression, observed for both mixers. Relative to a nominal ALMA band 9 mixers that are mounted onto ALMA cartridges, the SIS junction area of Chalmers produced SIS is up to two times larger. That results in up to twice the required LO power as well as √2 less magnetic field that is required for optimal noise suppression. The largest expected effect is on maximum IF frequency.

Measured heterodyne noise temperature is presented in Figure 12. From the first attempt, we were able to obtain noise as low as the best ever ALMA band 9 mixers. The mixer number 606 (junction area of 0.8 μm^2) performed the best in the first test. We have chosen junctions from the same junction size design and measured them as well (see Figure 12). The curves lie on top of each other. From these very low-number statistics, we can nominally conclude the RF yield has a good potential and is much larger than the RF yield we have registered during ALMA production. The RF yield does include an ability to suppress the Josephson noise using magnetic field. It is this criterion that was the main reason for the relatively low yield of good mixers during ALMA production. The new mixers show smooth magnetic field tuning curves.

3.2.2 IF performance

The IF performance of a typical measurement for mixer 608 is shown in Figure 13. Overall, a low noise temperature with flat IF frequency response is demonstrated. There is an on-set of increased noise temperature at 10.5 GHz. The reason for this can be that we used out of specification 4-12 GHz isolators what can have a reduced performance towards 12 GHz bands. The mixers will be evaluated in the large IF band frequency cartridge using direct mixer amplifier connection. This can only be done in the next phase due to lack of resources. From these measurements, we conclude that current ALMA band 9 IF band of 4-12 GHz is adequately covered and there are good prospects to measure at the larger IF bandwidth. Results of calculations in Figure 22 also suggest performance degradation for frequencies above 12 GHz.

Figure 14 shows comparison of receiver gains vs. IF for new measured junctions in comparison with ALMA baseline design. Recent measurements from ALMA cartridge 41 have been used. The relative receiver gain was obtained by calculating receiver noise temperature vs. IF based on Y-factor measurements. Then the gain was divided by a minimum noise temperature from the same curve. To obtain the minimum, a 10-point moving average has been used before finding the minimum. Finally, curves corresponding LO frequency at the beginning, middle and top of the RF band have been averaged. Results in Figure 14 show, that we do have an onset of receiver gain degradation for new batch starting at between 8 and 10 GHz, with top receiver degradation is approximately 2dB. This may indicate either a problem with cryogenic isolator performance in our test cartridge (an out-of-specification 4-12 GHz isolator was used), or indeed a roll-off of the receiver gain due to parasitic capacitance, see results of the modeling in Figure 22. We plan to measure the new mixer's performance in our wide band IF set-up, which will help to isolate the problem with the performance. The new mixer still meets the ALMA specification with margin as data in Figure 12 represents the average over 4-12 GHz IF band.

3.2.3 Magnetic tuning performance

Magnetic tuning performance has been tested by performing scans of IF output power vs. SIS bias voltage for different magnetic coil currents, see Figure 15. The measurements were done at 660 GHz LO at around optimum LO power. Josephson noise feature is clearly seen in the picture. It is also the first minimum visible at 7 mA and second minimum at 10mA, and their counterparts with negative values. Note that "0" value is shifted to 2mA due to hysteresis in magnetic VACOFLUX® core. From these measurements, it is clearly enough bias region to operate the mixer already staring at the first minimum. Also, the Josephson current suppression profile is consistent with the round shape of the junctions.

We did not consider custom junction shapes, such as rectangular or rhomb shapes. The mentioned shapes required extra effort to be accurately reproduced on the chip and would have demanded using e-beam lithography, while the Josephson current suppression curve would have sharper minima, that is more difficult to find in an automatic tuning. Round junctions are easy to produce, require less definition resolution and have relatively shallow minima of Josephson current vs. magnetic field strength.

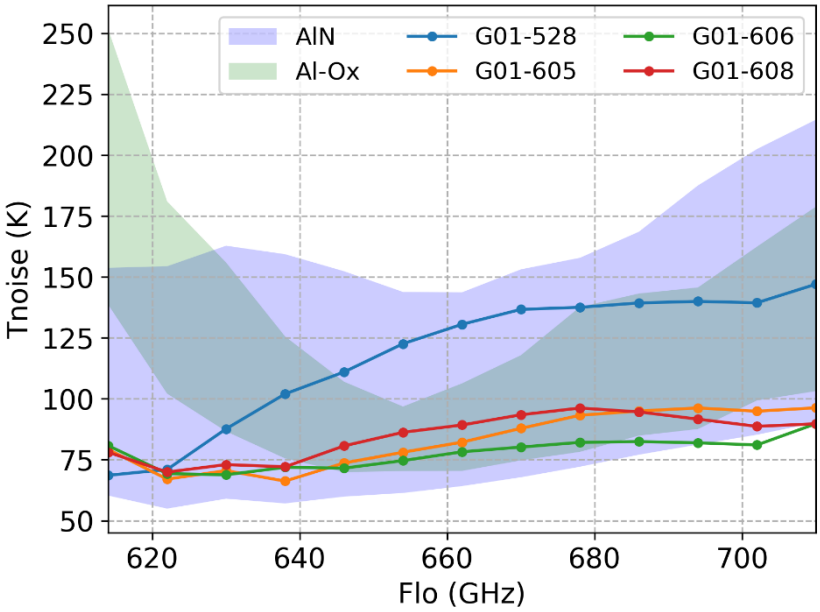


Figure 12. Measured total IF band (4-12 GHz) noise temperature with respect to LO frequencies. Results contain curves for all 4 mixers measured with the background of results from all 73 ALMA receivers, separated by the SIS junction's technology. Shaded areas represent the area between minimum and maximum noise temperature of ALMA cartridges. G01-528 has a larger SIS junction area than G01-605,606,608.

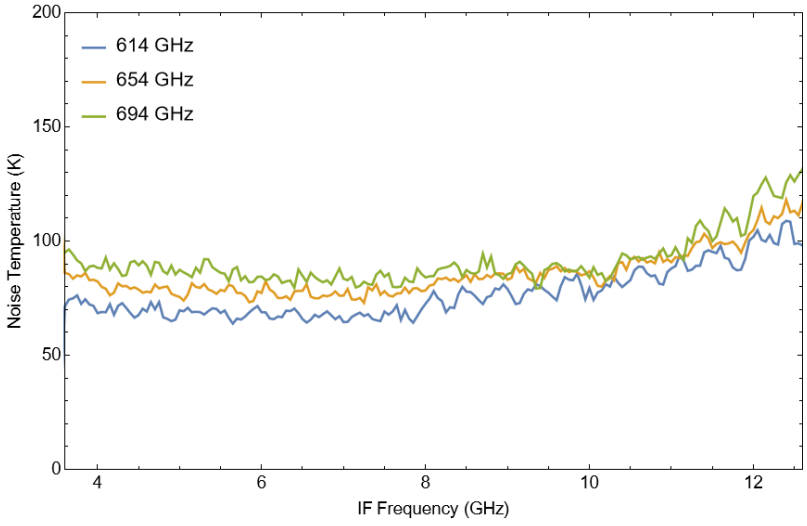


Figure 13. Measured receiver noise temperature vs. IF frequency for three LO frequencies.

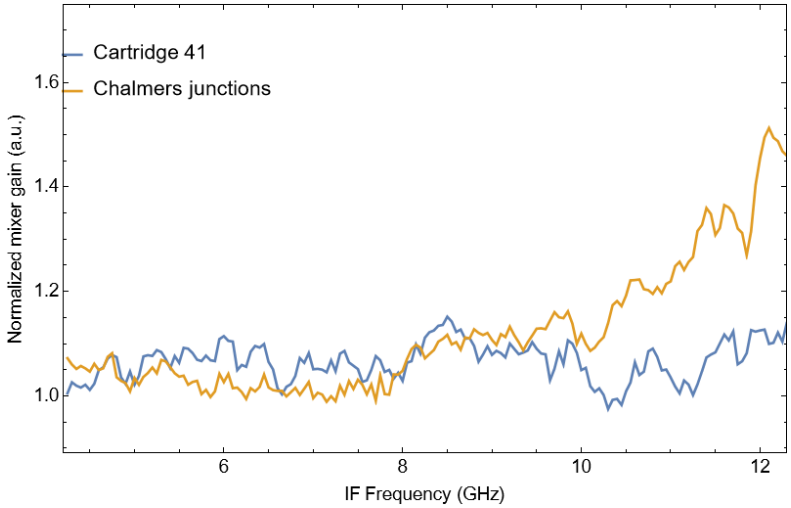


Figure 14. Comparison of normalized mixer gain vs. IF for mixer from Chalmers, compared with mixer gain from cartridge 41 as representative of old batch. See text for the explanation.

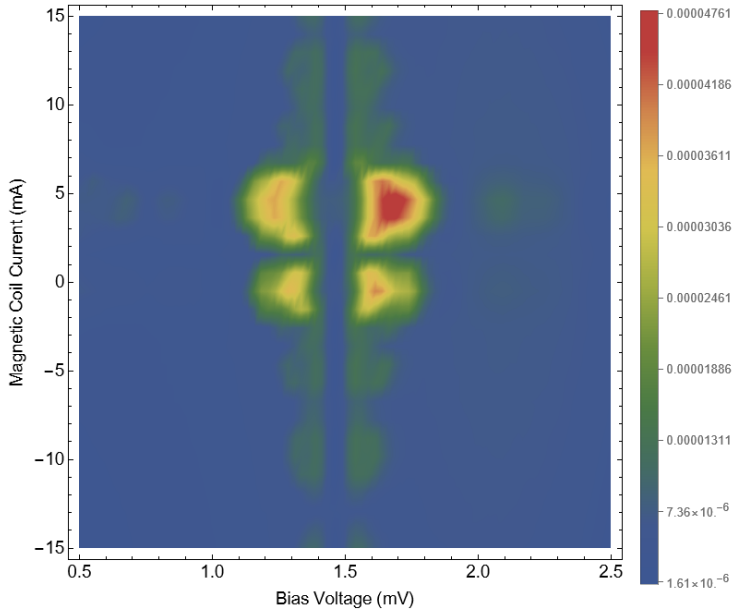


Figure 15. Measured IF output power at 6 GHz vs. SIS bias voltage while stepping through magnetic field current. Color is in linear scale.

3.2.4 FTS response measurements

The Fourier transform response measurements have been performed in a separate liquid helium cryostat. The Michelson interferometer scheme has been used to measure the spectrograms. Mixers 528 and 606 have been measured. This type of measurement is especially useful to evaluate the total RF bandwidth of the SIS mixer. Results for mixers with different junction areas are shown in Figure 16. It is clear that the larger area mixer's response is shifted to lower frequencies and that the lowest frequency is limited by the waveguide cut-off. Generally, ALMA Band 9 RF band (602-720 GHz) is covered with sufficient margin for both designs. The picture for Figure 16 corresponds well with noise

temperature curves shown in Figure 12 which clearly demonstrates better performance of mixer 606 at higher frequencies.

During ALMA band 9 production project, we measured the effect of mixer response reduction at higher frequency due to suppression of superconducting gap in high magnetic field. This happens due to proximity effect in Al-Nb interface in the tuning structure microstrip lines' bottom layer. This can be clearly observed by measuring an FTS response for different magnetic fields. This type measurements for sample 606 is shown in Figure 17. The effect is clearly visible. For the new junctions, we expect the effect to be smaller because larger junctions need lower magnetic field to achieve the Josephson current suppression.

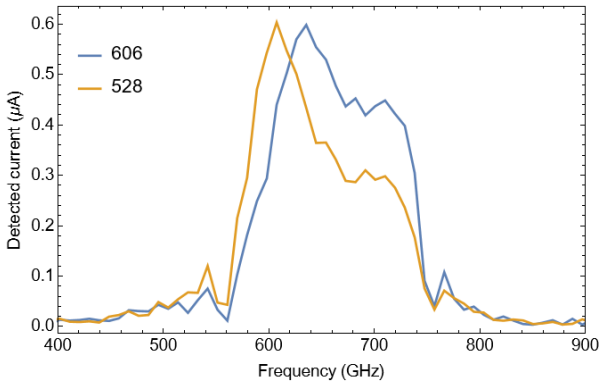


Figure 16. FTS direct detection response for two mixers 528 (larger area) and 606 (smaller area). Measurement is done at magnetic field coil current of 3mA.

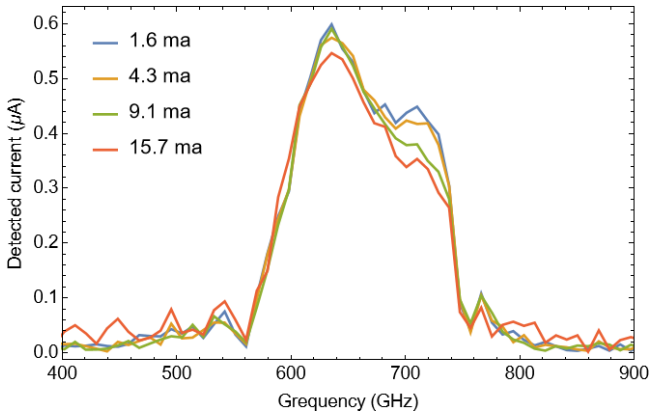


Figure 17. FTS direct detection response for mixers 605 measured at different magnetic field coil current shown in the legend. The proximity effect of superconducting gap suppression at higher frequencies and higher magnetic field is clearly visible.

3.3 Analysis of performances of the Band 9 SIS mixer demonstrator and comparison with simulations

3.3.1 Optimization parameters and results

To utilize cost effective and efficient demonstration of GARD SIS technology for ALMA band 9, we have decided to leave all waveguide dimensions constrained and only modify geometrical dimensions of an on-chip integrated tuner. The design of single SIS junction with an end-loaded stub followed by two-stage microstrip transformer and bowtie waveguide probe remain fixed as well. Since the main

challenge of re-optimization is to increase junction area towards requirement of technology, it has been decided to stay with a single junction design, because dual junction will reduce normal resistance even further in comparison with already low normal resistance of large current density single SIS device. Single junction design also allows to avoid SQUID-like effect with very fine structure of SIS critical current vs. magnetic field dependence, which makes it difficult to suppress Josephson current in SIS mixer. This suppression is a requirement for ALMA band 9 frequencies to achieve stable low noise SIS mixer operation. Other chip parameters remain fixed at values used to evaluate typical ALMA band 9 mixer design.

Optimization has been done using full 3D EM analysis in Microwave Studio package. The 3D model includes models of dielectric with losses, material model of superconductor metal structure with kinetic inductance and losses included and model of SIS junction represented by a lumped element port with real part of SIS junction impedance and lumped element capacitor representing SIS junction capacitance. The geometrical parameters of all defining microstrip transformers, waveguide probe and RF band rejecting filters and waveguide structures have been included in the model as parameters. The absolute match |S21| between waveguide input port and SIS junction port has been calculated over required frequency range, to evaluate performance. The first initial set of parameters for nominal design has been evaluated to check the model. Then SIS junction area has been increased stepwise 0.5->1>2>3 um^2 and at each step a parametric search (gradient optimization) has been performed with maximizing |S21| parameter in the required frequency range. This produced a set of parameters producing graphs as put into report. For this optimization we did not change the current principle of junction matching, i.e. end-loaded stub with two-stage transformer between SIS junction and waveguide probe as we are confident that this design works well with small junction area. It also became clear that it is the junction capacitance that limits IF performance in absence of external IF tuning circuit. If we were to add external tuning circuit and/or RF mechanical structure this would lead to complete redesign of the mixer, which was not the intention. We intend to design a drop-in replacement for our current mixer block. For underlying principles of MWS studio calculations one can be referred to the user manual.

As discussed before, we would like to re-optimize the current successful ALMA band 9 SIS mixer design for much larger SIS junction area. We have done optimization for 1 μm^2 and 2 μm^2 (process best-effort).

It was possible to find suitable layout geometries to achieve a good match throughout the RF band. Optimized mixer layout is shown in Figure 18 for both junction areas. It is clear that, despite the tuning overlap area decreases for larger junctions, the total circuit overlap area increases with increase of SIS junction area which we will see back in IF performance of the designs, see the last column in Table 4. Figure 19 presents equivalent circuit layout to the extent the 3D distributed elements can be mapped to a lumped element/stripline representation. As in the scheme, the absolute RF coupling can be calculated as |S21| and IF coupling |S23| while using RF impedance and IF impedance for port 3 reference impedance. C_{SIS} is calculated from specific capacitance and junction area. RF impedance is calculated from RnA product and junction area. The rest of parameters are related to 3D model.

Calculated input match for layout configurations in Figure 18 is shown in Figure 20. Good band coverage can be achieved for both junction sizes. The input match has also been calculated for ± 20% of junction area for small junction and ±10% for large junction, realizing that linear dimension tolerances would be independent upon junction's area. It is clear that both design configurations are

robust with respect to junction area variation, which is the main uncertainty in SIS junction production process. The overall matching curve shape is very similar for both junction areas.

The calculated output IF match for both design configuration is shown in Figure 22. SIS mixer output match calculated for optimum layouts: old 0.65 μm^2 area (blue), 1 μm^2 junction area (green), 2 μm^2 junction area (red), 3 μm^2 junction area (magenta). Layout from Figure 17 was It is clear also in comparison with baseline ALMA band 9 design, that IF performance is degraded both in terms of 3dB IF bandwidth as well as in terms of absolute match figures. ALMA specifications on the 4-12 GHz IF bandwidth is likely still to be met with sufficient margin, the noise performance is expected to degrade by 10K for a smaller junction and by 20K for a larger one on top of a 100K typical DSB noise. Numbers calculated for an amplifier noise temperature of 5K and mixer conversion gain of 3dB. The increased noise temperature will still be well within ALMA band 9 specifications.

The input noise temperature can be present as a sum of mixer noise temperature T_{mix} and an IF amplifier contribution T_{amp}/L_{mix} , where T_{amp} is IF amplifier noise temperature and L_{mix} is mixer conversion gain. Although the exact value of L_{mix} can only be calculated from Thucker theory which requires much more effort, the mixer output match can be estimated from microwave theory as S23 parameter in our model. When S23 parameter is changing by 3dB as evident in the figures, the IF amplifier contribution will increase correspondingly. The nominal design mixer conversion gain is -6dB (as estimated) and IF amplifier contribution would be 20K. If that gain is decreased by 3dB the amplifier contribution increases by 10K. The number is an estimate with assumptions given above and depends on IF and LO frequency.

Table 4 below summarizes parasitic IF capacitance of tuning structure compared to capacitance of SIS junction itself. As junction area increases, the parasitic IF capacitance also increases limiting IF bandwidth according to Fano-Bode theorem. This effect is clearly visible in IF match calculation in Figure 18. SIS junction on-chip layout: a) central part of the chip optimized for 1 μm^2 junction area, b) central part of the chip optimized for 3 μm^2, and c) general layout of the circuit in the waveguide, which is similar to baseline ALMA band 9 design. Rose color is top Nb layer, violet color is bottom Nb layer. SiO_2 substrate is depicted in green color.

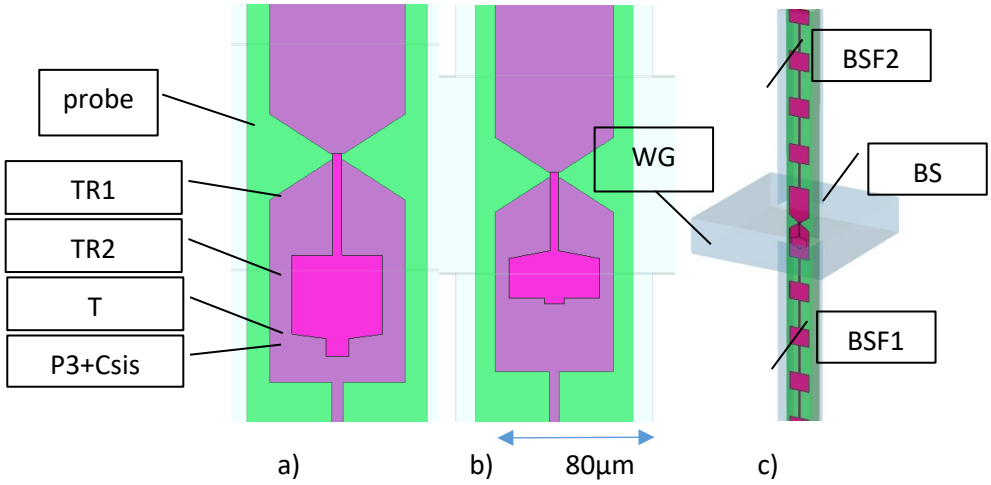


Figure 18. SIS junction on-chip layout: a) central part of the chip optimized for 1 µm² junction area, b) central part of the chip optimized for 3 µm², and c) general layout of the circuit in the waveguide, which is similar to baseline ALMA band 9 design. Rose color is top Nb layer, violet color is bottom Nb layer. SiO_2 substrate is depicted in green color.

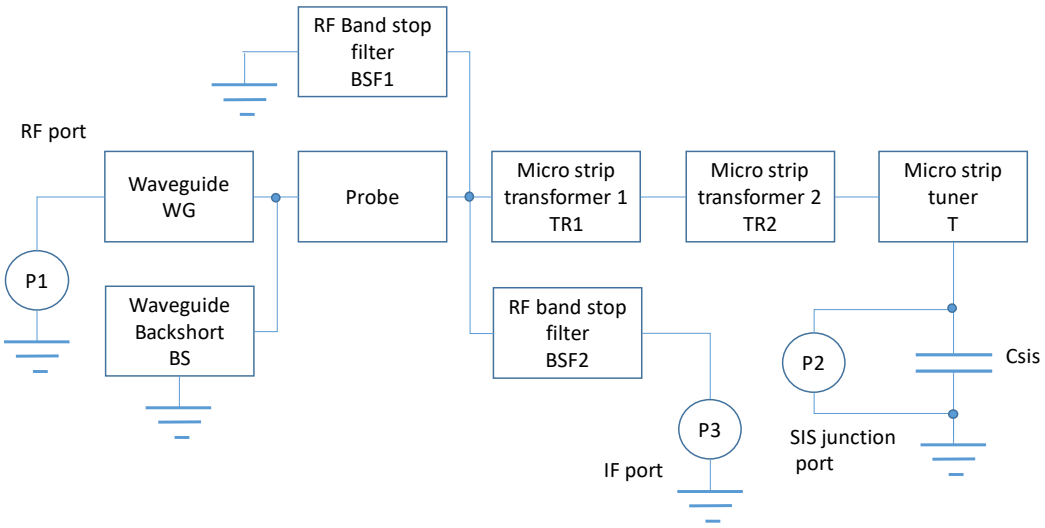


Figure 19. Equivalent circuit representation of calculated design. P1 is waveguide RF port, P2 is SIS junction port, P3 is IF output port. Equivalent layout elements presented in Figure 18.

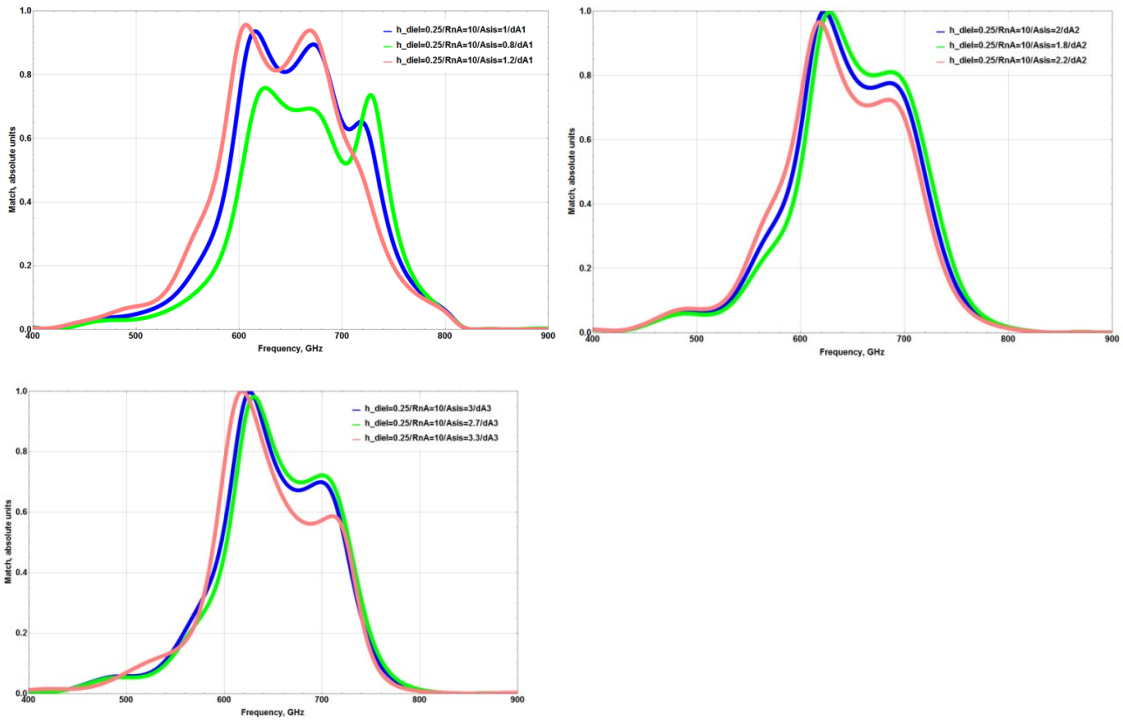


Figure 20. SIS mixer input match calculated for optimum layouts: top left optimized around 1 μm² junction area, top right -- optimized around 2 μm² junction area, bottom left optimized around 3 μm² junction area. Junction area has been varied for both cases as indicated in figure legends.

Table 4. Parasitic IF capacitance of tuning structure compared to capacitance of SIS junction itself.

name	A_{sis},μm^2	A_{idle},μm^2	$C_{(idle-Asis)}$,fF	C_{sis},fF	C_{tot},fF
A_3	3	1198	160,828	255	415,8
A_2	2	1160	155,848	170	325,8
A_1	1	1578	212,239	85	295,2
A_{old}	0,5	604,2	81,2483	30	111,2

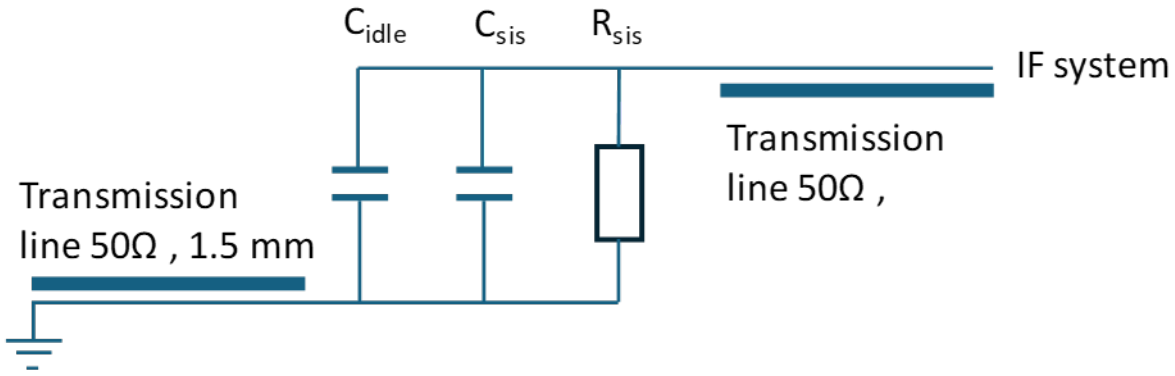


Figure 21. Equivalent circuit representation of calculated design at IF frequency.

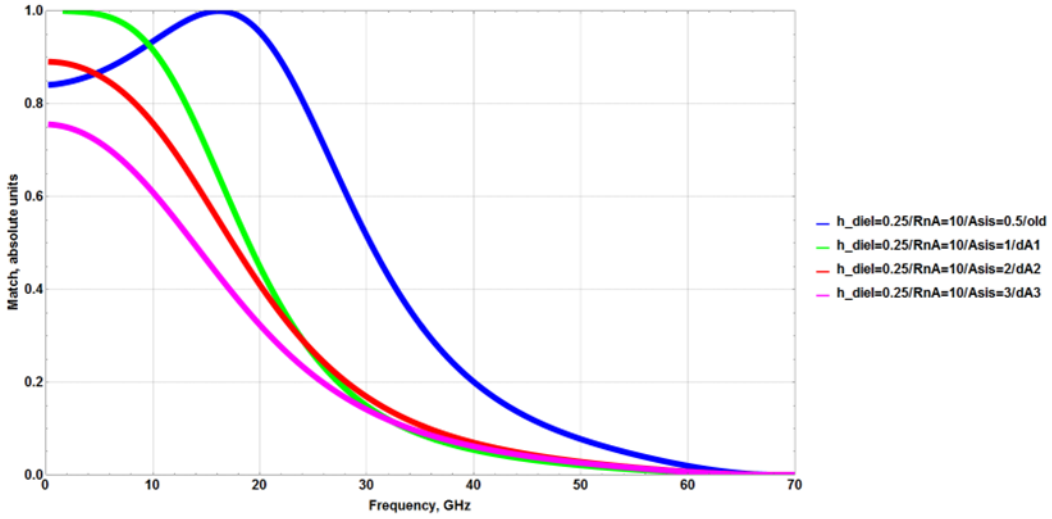
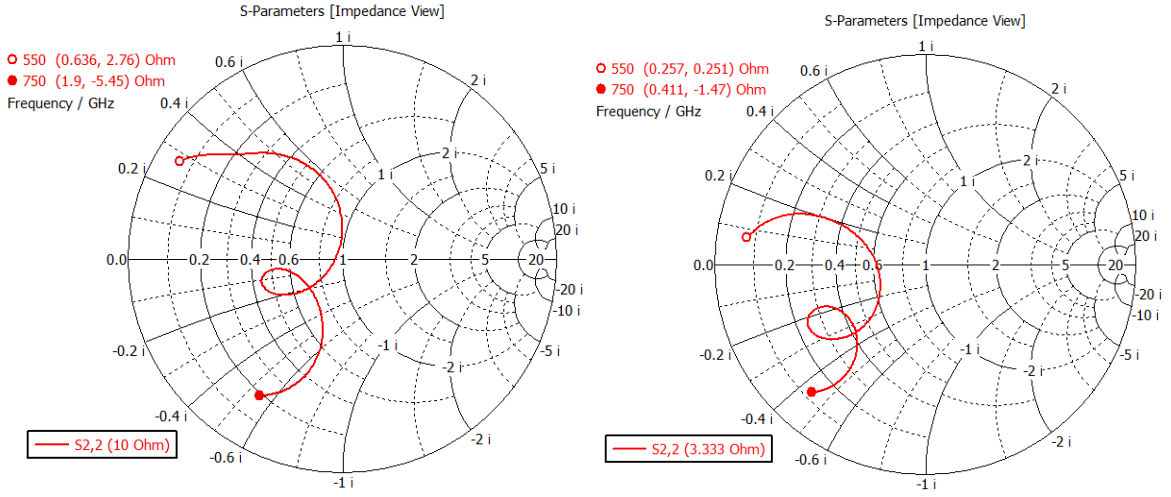


Figure 22. SIS mixer output match calculated for optimum layouts: old 0.65 μm² area (blue), 1 μm² junction area (green), 2 μm² junction area (red), 3 μm² junction area (magenta). Layout from Figure 17 was used.



a) b)

Figure 23. SIS mixer embedding impedance: a) optimized around 1 μm² junction area, b) optimized around 3 μm² junction area.

Calculated SIS junction embedding impedance is shown in Figure 23. For both design optimization embedding impedance curve occupies stable SIS operation region which manifests absence of potential negative dynamic resistance of SIS junction at operating point.

3.3.2 Performance discussion

By comparing calculation sets in Figure 20 with FTS measurements of Figure 16, we can see the FTS response resembles the calculated mixer coupling. Note that there are many parameters that can vary in SIS mixer production, both in thin film processing and in further mounting and polishing steps. In addition, we note that the desired design R_nA value is 10 Ω·μm² and the new batch has R_nA value of 13 μm² which can also account to difference that is observed. The most straightforward way to estimate the impact of different RnA is calculate RF coupling degradation using impedance mismatch formula. The mismatch due to R_nA is 98% so it would correspond to a negligible 2% noise temperature improvement. There is also a clear shift in tuning of the mixer. The best match to the FTS curves clearly corresponds to a 2 square micron junction area. This may happen due to underestimate of inductance of tuning structure. If there is a desire to improve the performance further, we need to perform modeling/optimization development cycle with Chalmers technology.

The IF performance simulated in Figure 22 shows that we do expect IF performance degradation for larger area junctions. So, ultimately, we need further iteration to decrease the junction area, which goes beyond the scope of the current project. Additional measurements would be needed to establish the high IF frequency limit of the current design.

3.4 Conclusions

We have redesigned a baseline ALMA band 9 mixer to adhere to manufacturing capabilities at Chalmers University. The corresponding mask design has been created and SIS junctions have been manufactured at Chalmers and then diced and mounted to ALMA band 9 mixers at NOVA. The DC evaluation of SIS junction has demonstrated 80% DC yield and very high quality of I-V curves. Heterodyne evaluation demonstrated excellent RF performance and repeatability of the mixer

performance, showing RF yield closer to 100% (based on low number). The new mixer covers at least IF band of 4-12 GHz and performs better than most of ALMA band 9 production batches. Further improvement of mixer performance is possible as well as further tests in 2SB and wide band configuration is desired.

To make the design compatible with WSU upgrade specifications the following steps are envisaged:

- Make measurement of current design in a wide band IF system (4-20 GHz) and analyze the IF response.

- Make device layout optimization for high IF frequency, that includes CST simulation and may require 0.5 square micron junctions. Optimization should Chalmers technology design rules.

4 Summary

In this report, we have presented the SIS fabricating process developed targeting to suit the requirements set by ALMA for its next generation receivers. The AlN tunnelling barrier of the SIS allows achieving lower specific resistivity of the junctions without compromising of their quality along with the reduced specific capacitance – both compared with the standard AlOx -barrier junctions. Along with that, the junction area was demonstrated to be pressed down to the submicron.

The Band 9 demonstrator mixer equipped with the 0.8 μm^2 Nb/Al-AlN/Nb SIS devices fabricated with the developed process demonstrate the state-of-the-art noise performance. The potential was demonstrated to press further the area of the practical SIS junctions probably down 0.5 μm^2.

Additionally, the same developed SIS process served another ESO study [22] with SIS mixer devices for the Band 6/7 band and the first results [23], [24], also presented recently at the ISSTT2024, have also shown the suitability and usefulness of the developed process.

Summarizing, the updated SIS fabrication process, which is the subject of the present report, proves its suitability and advantage for use in the coming ALMA receiver upgrades.

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