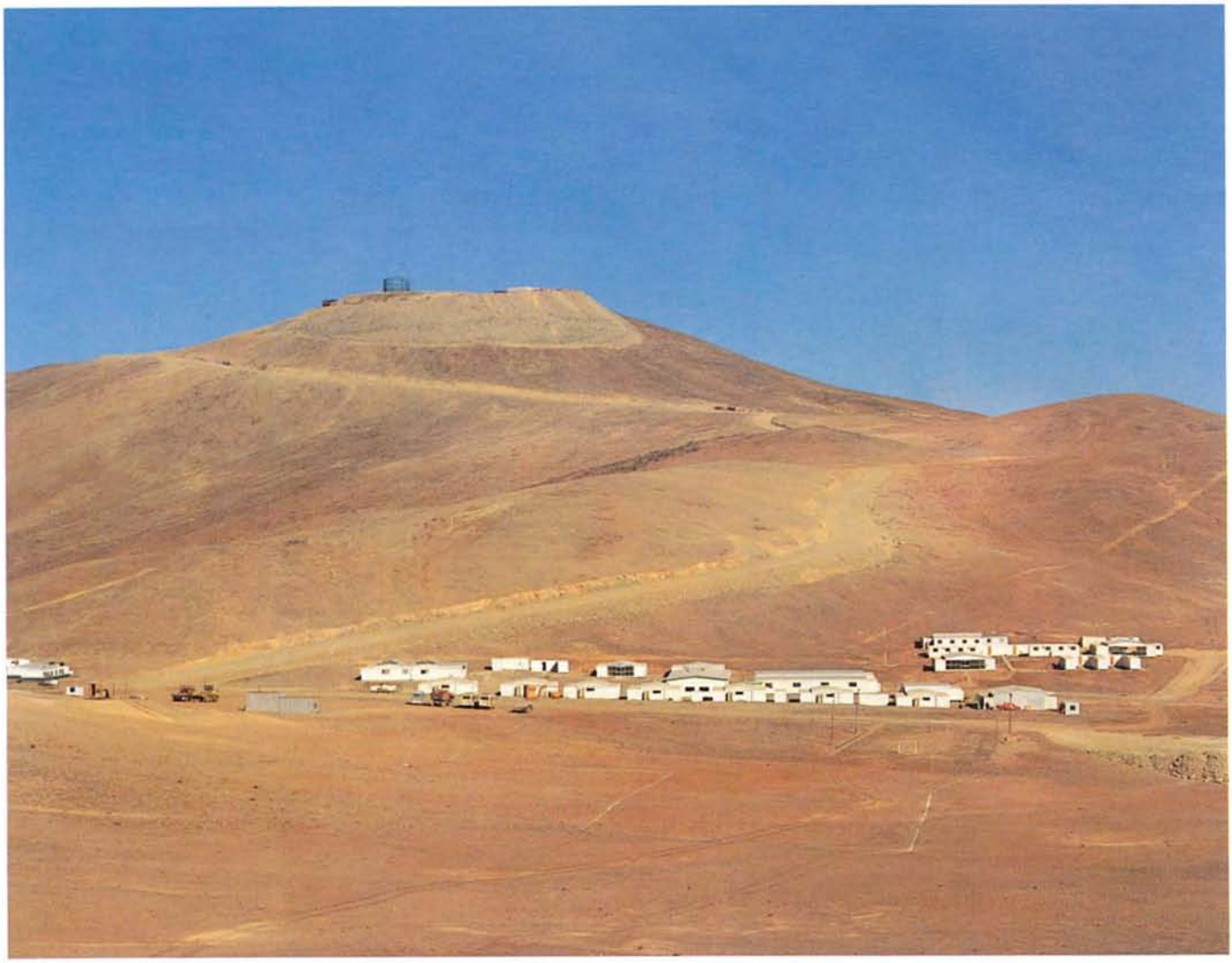

Figure 3.

tion of the assembly of the enclosures as well as of the telescopes. Near the soccer field in the foreground of the picture we will soon start the construction of the building that will be used for the aluminisation of the primary mirror and for the construction of the other technical complexes necessary to operate the new ESO Observatory. One of these technical buildings will accommodate the power generators that will produce the necessary electrical power. A contract with the company CEGELEC is about to be signed for this important and vital unit.

The Plan for Optical Detectors at ESO

J. BELETIC, ESO-Garching

1. Introduction

In January 1995, ESO gave increased emphasis to optical detectors by establishing the optical detector group within the Instrumentation Division. This restructuring was intended to provide the resources necessary to significantly improve ESO's technology in optical detectors. In addition to this group in Garching, there are several other persons, including a group of engineers at La Silla, that work on optical detectors. In order to co-ordinate our efforts, we have organised into the Optical Detector Team (ODT) and we have defined a strategy for our work. These plans have been reported to the Scientific Technical Committee (STC) and the User Committee (UC) and we have received their support. The intent of this article is to present our plans to the whole of the ESO community.

2. Our Vision

Our plans are guided by the following technological developments:

CCD devices are becoming nearly perfect detectors of optical radiation; high quantum efficiency devices can be made for wavelengths from the atmospheric cut-off at 300 nm to ~1000 nm.

Readout amplifiers for CCD devices have improved so that it is now possible to attain less than 2 electrons noise at "slow" readout rates (100 kpixel/sec/port) and 4–6 electrons noise at 1 Mpixel/sec/port.

It is possible to build electronics today that can run any CCD detector or mosaic of detectors that we can envision for the next 10 years.

Our vision is for ESO to have detector systems of high quantum efficiency, low

noise and fast readout. While fast readout is only mandatory for a few applications, such as adaptive optics and rapidly varying phenomena, high speed will make nearly every instrument more efficient. Acquisition, focusing, direct imaging and calibration data collection will greatly benefit from high-speed readout. Also, the ability to read and display images quickly will be a significant advantage during instrument integration and testing.

3. The Present Status of ESO's Optical Detector Systems

CCD detector systems are made of three basic components: CCD chips, cryostats and the CCD control electronics. At La Silla, there are backside-illuminated, high quantum efficiency (q.e.) CCDs at all instruments, with the exception of the B&C and EFOSC2. B&C is being upgraded in March 1996 and we are working with the astronomy department in Chile to define the proper time to upgrade EFOSC2.

We will always strive to obtain better CCDs, but at present the major weakness of our systems is the control electronics. The CCD controllers that are presently in use on La Silla, named the "VME controllers", are among the poorest functioning controllers of any major observatory. The standard readout rate is 15 kpixels/sec, the electronics suffer from a myriad of noise problems, and the system has internal crosstalk that prohibits use of more than one readout port. Consequently, the VME systems read slowly with relatively poor noise and occasionally suffer more dramatic problems. The La Silla detector engineers should be given credit for maintaining and optimising these systems as well as possible.

In order to remedy this situation for the VLT instruments, a new-generation CCD controller has been under development at ESO for several years. The ACE (Array Control Electronics) system provides a significant enhancement over the VME: better noise performance and reading of multiple ports to rates of 90 kpixels/sec/port. Fundamentally, there is nothing wrong with ACE, except that its specification will be outdated for future applications. ACE is not capable of operating the new generation of high-speed, low-noise CCD devices to the fullest of their capabilities.

4. Primary Development Effort Through 1996 – Advanced CCD Controller

ESO must produce many CCD systems in the next few years in order to provide for the VLT instruments and to upgrade La Silla. The most sensible approach is to produce a single "universal" controller that can operate all of ESO's CCD devices. This saves money and time in production, maintenance and training. Since the ACE controller can not satisfy the readout requirements of the new generation CCD devices, the optical detector team has started a parallel development effort for an advanced CCD controller.

We are pleased to report that the advanced CCD controller development has proceeded very well since we began this effort in the second quarter of 1995. We have established a system architecture that should be able to run any CCD chip or mosaic that is foreseen through the year 2005. The advanced controller will be able to operate up to 32 readout ports at multi-MHz pixel rates (per port), and all major parameters will be fully programmable. The system design goal is to have performance limited only by the CCD device and the imagination of the user. Thus, the system can be run slowly to get the very lowest noise (< 2 electrons) for long-exposure faint spectra or run fast (expect 4–6 electrons noise at 1 Mpixel/sec/port) for acquisition, focus, calibration or direct imaging. The advanced controller has been given a name: FIERA (Fast Imager Electronic Readout Assembly). Proposed by our Chilean staff and voted in by the ODT, FIERA has the meaning "wild animal", such as a lion, in both Spanish and Italian. The specifications for the FIERA controller are listed in the box below.

We are applying most of our research and development energies to FIERA through 1996 so that the development

Specifications of the FIERA CCD Controller

The fundamental goal for FIERA is to make a controller that can optimally operate any CCD chip or mosaic that ESO acquires for the next 10 years. The limitation of the entire detector system should be due solely to the CCD and the imagination of the user. The electronics (hardware and software) of FIERA should be transparent to the user. Later this year we will publish an article on FIERA after we complete the prototype testing. We list here some of the specifications of the FIERA design:

- *50 MHz fundamental clock*
- *Up to 32 readout ports*
- *Up to 50 Mpixel/sec total*
- *Up to 21 bits/pixel*
- *Up to 5.5 Mpixel/sec/port*
- *Initially 1 MHz pixel rate limitation at 16 bits per pixel (set by A/D limitation)*
- *Readout noise must be dominated by the CCD device for both slow and fast readout; the electronic noise must be negligible*
- *Fully programmable high-current clock drivers (25.5 V swing, 0.1 V resolution at 50 MHz, 2 amps instantaneous per driver)*
- *Nearly unlimited number of control bits (at 50 MHz)*
- *Analogue biases fully programmable with hardware limits on potentially damaging biases*
- *4 gain settings*
- *64k offset levels*
- *4 low pass filter settings (can optimise clamp & sample at 4 speeds)*
- *Gbit/sec fiber optic data link from detector head to embedded computer*
- *Embedded telemetry and test signals*
- *No software in the detector head / minimalistic design*
- *Fully modular and expandable.*

The FIERA controller consists of three modules:

- *A set of detector head electronics that will be mounted as close to the CCD as possible, preferably on the CCD cryostat itself. (If there is too much distance between these electronics and the CCD, we will use pre-amplifiers to boost the video signal for low noise performance.)*
- *A DC power supply module that generates a set of clean voltages for the detector head electronics. This power supply should be within 3 metres of the detector head electronics.*
- *The detector computer with a custom-made computer interface board. The interface board contains a Gbit/sec duplex fiber link and two C40 DSP chips for system control and interface to external computers/processors. The distance of the fibre-optic data link between the detector computer and detector head electronics can be up to 500 metres with standard parts, up to 20 km with pin compatible upgrade to more expensive transmitter/receivers.*

For the system we only need to custom design six printed circuit boards; the computer interface board and five boards in the detector head:

- *communications board (fiber link and bus interface)*
- *clock drivers*
- *analogue biases*
- *video processing (amplification, gain, offset, correlated double sampling, digitisation)*
- *custom backplane*

A good feature of the system is that there is no software or processors in the detector head. The detector head runs via an "extended bus" structure provided by the Gbit/sec data link. All system "smarts" reside in the C40 sequencer chip and the SPARC computer that is used as the dedicated computer for the system.

process follows an accelerated schedule. We are being assisted in the development by two ESO member institutions: (i) Roma Osservatorio has provided a staff member to work part-time in Garching, (ii) University Copenhagen has provided a "tiger team" for design review.

The first FIERA prototype will be running in May 1996 and we plan to take the remainder of 1996 to iterate on the hardware design and to write the control software. Production and deployment will commence in January, 1997. Since the FIERA development schedule has become a tangible reality, all instruments with detector deliveries starting in 1997 have given their approval to using FIERA for their detector systems.

The ACE system, which was successfully tested at the NTT in January 1995, is now completing final design changes and it will be used as the controller for the FORS 1 instrument delivery in March 1996. We will also use ACE for the Big-Bang upgrade in the second half of 1996.

5. CCD Procurement

In parallel with controller development, ESO is procuring the best of the new generation of CCD devices. In Table 1 we indicate the specifications of the kind of devices that we are looking for.

We are seeking two different CCD sizes with the qualities indicated in the Table:

- 2k × 4k, 15-micron pixel, 3-side buttable device with 2 readout ports along the 2k side. For use in scientific instruments as single devices or in mosaics. In many cases (e.g. SUSI-2, FUEGOS), there will be two devices in a 4k × 4k mosaic.
- 128 × 128, 25-micron pixel, split frame transfer device with a total of 16 readout ports (8 top, 8 bottom). For use in the NAOS adaptive optics system, but also may be useful for VLTI.

At present, we are involved in a preliminary enquiry to gather information from prospective manufacturers and we aim to have a procurement in place around the end of first quarter 1996.

We are pursuing a second source for 2k × 4k detectors via a consortium to obtain CCD chips from MIT Lincoln Laboratory (MIT/LL). MIT/LL produces some of the best CCDs in the world. Their devices have consistently established the lowest readout noise at rates from 50 kHz to 5 MHz and MIT/LL has much experience with thick devices with high q.e. in the near infrared. The contract with MIT/LL will produce a limited number of devices, but we expect to get high-quality thinned devices on both standard silicon and thick, high-resistivity silicon. These devices are the first choice for the red arm of UVES.

We have also initiated a contract with Mike Lesser of the University of Arizona to produce three thinned VLT test camera chips and four more thinned 2k × 2k, 3-side buttable, 15-micron Loral devices. With a number of thinned Loral 2k × 2k devices already in stock at ESO, we have CCDs that are presently first choice for UVES blue, backup for UVES red and are appropriate for upgrades at La Silla. The VLT test camera CCD, which was designed exclusively for ESO, has a 2k × 2k, 24-micron, 4-port array with four small "tracker" chips at the corners. The compatibility of the VLT test camera device with the Tek/SITe 2k × 2k devices gives the advantage that each kind of CCD serves as a backup option for the other.

We have a small contract to obtain two Philips 7k × 9k, 12.5-micron arrays from the first lot of CCDs ever made by filling the width of a 6-inch fabrication wafer with pixels. The first devices will not be suitable for scientific application since these are front-side devices with a vertical anti-blooming drain that limits sensitivity to 400–900 nm and a peak q.e. of 28%.

6. Cryostat Developments

ESO has been developing two kinds of cryostats for use with the CCD systems: (i) a bath cryostat, which has a tank of liquid nitrogen with hold times of over 2 days, and (ii) a continuous-flow cryostat that, via feed from a 100 litre liquid nitrogen tank, can keep a CCD chip cool for over two weeks. Both types of cryostats have been designed to work with the same detector head, which is removable from the cryostat body.

The new bath cryostat design was tested in January 1995 at the NTT, and during 1995, a total of 10 detector heads and 5 bath cryostat tanks were produced. One complete system has been fully tested for integration with the FORS 1 CCD. During 1996, the bath cryostat for the VLT test camera will be integrated and tested. The continuous-flow cryostat prototype has been given a thorough test at the CES facility and during 1996, the two continuous flow systems for UVES will be fabricated.

During 1996, we will begin work on thermoelectric cooling of the NAOS wavefront sensor CCD devices.

7. La Silla Upgrades

Test time has been granted February 29 – March 8, 1996 to upgrade the B&C spectrograph on the ESO 1.5-m telescope. We will install a Loral / U. Arizona 2k × 2k, 15 micron CCD chip that has high quantum efficiency (q.e.) in visible and UV, as demonstrated by the new CES chip.

Upgrade of the B&C will leave one last low q.e. device on La Silla, in EFOSC2 at the 2.2-m telescope. We plan to use another Loral / U. Arizona 2k × 2k to upgrade EFOSC2. At present, a definitive date has not been established for this upgrade, as this upgrade must be co-ordinated with the potential move of EFOSC2 to the 3.6-m telescope.

As part of the NTT Big Bang, we will upgrade the electronics of the SUSI and EMMI detectors to the ACE/LCU systems in November 1996. These systems will provide readout rates to 90 kHz out of 2 ports for the CCD devices on SUSI and EMMI. Depending on the noise vs. speed performance of the CCD devices, this will enable a sixfold decrease in readout time. The days of 5-minute readout of the EMMI Red 2048^2 CCD are numbered.

8. Schedule of Deliveries of Detector Systems to Instruments

In addition to the La Silla detector upgrades (B&C, EFOSC2), the ODT has taken the following commitments for optical detector system delivery:

1996 March FORS 1
ACE/LCU plus eng. grade Tek/SITe 2k × 2k

1996 July NTT
3 ACE/LCU systems (no new cryostats or CCDs). Telescope integration November 1996.

1996 December FORS 1
Put science grade device and final version of all electronics into the system.

TABLE 1. Specifications of the new CCD devices required by ESO

Very low noise at "slow" readout rates (50–100 kHz) – goal is 2 e^- or less
Moderate noise at 500 kHz – goal is 3–4 e^-
Fairly good noise at 1 MHz – goal is 4–6 e^-
High q.e. from 300 nm through 1000 nm, specifically

Wavelength	320	350	375	400	450	500	600	700	750	800	900	1000
q.e. (%)	70	70	70	80	80	85	85	80	75	70	50	15

Very good cosmetic quality and high charge transfer efficiency

(The term kHz refers to kpixels/sec/port, and MHz means Mpixels/sec/port; a CCD chip or a mosaic may have many ports operating in parallel.)

1997 June VLT Test Cam #1
FIERA with thinned chip (2k × 2k + tracker chips). We may need to deliver this system earlier.

1997 July UVES
FIERA blue arm (2k × 2k eng. grade device).

1997 September SUSI-2
FIERA with UV-sensitive 4k × 4k (two 2k × 4k devices).

1997 September NAOS
FIERA with AO chip (128 × 128), plus spare system (thermo-electrically cooled dewar).

1998 January UVES
Upgrade blue arm to science grade, deliver red arm 2k × 4k (single chip or mosaic of 2k × 2k), plus spare parts. If possible, we will deliver the red arm with the long-term goal of a 4k × 4k mosaic. In addition, the blue arm may be outfitted with a new generation 2k × 4k device.

1998 March FORS 2
FIERA with Tek/SITe 2k × 2k.

1998 March FUEGOS
FIERA with eng. grade 4k × 4k (two 2k × 4k chips).

1998 December VLT Test Cam #2
FIERA with thinned chip.

1999 March FUEGOS
Put science grade devices into system.

The ESO community should note that we are taking the position that all new CCD controllers on the VLT and new ones on La Silla (under ESO maintenance) will be FIERA systems. We take this stance because we have the responsibility to maintain all optical detector systems. In addition, ESO instruments should get the benefit of the advanced capabilities provided by FIERA. (This statement does not include the new system at the Danish telescope or FEROS, since FIERA will not be available until 1997.)

9. One Observatory – La Silla and Garching

The ODT has made great strides in improving communication between Garching and La Silla. One aspect is weekly video conferences on every Thursday. In addition, we plan for more personnel exchanges – at least one visit per year of each member to the other site for functional work. Also, all large development projects are now a shared concern, both for design and for maintenance – no more dichotomy of developing in Garching and giving to La Silla for maintenance.

FIERA is a first big step in this area. The second step we have taken is a "universal" temperature/vacuum sensing & temperature control box that will be used with VME, ACE and FIERA systems. This system is being developed in La Silla with interaction by Garching staff.

The third design area where we are combining efforts is a new CCD detector testbench. All members of the ODT will contribute to design and critique the development as it progresses in 1996.

10. Communication with the ESO Community – World Wide Web

We have taken the approach that the World Wide Web is the best avenue for communicating information to the ESO user community. A new, clearer and more concise presentation of data about ESO's CCD devices went on-line in the beginning of September 1995. Besides providing standard data, we use this medium for user requests. This information will continue to evolve as we receive comments and constructive criticism about the content and format. Please assist us with continual improvement.

11. Facilities

A new facility upgrade planned for 1996 is the design and construction of a new CCD testbench. With an increased number of new detectors and the old testbench dependent on the VME controller, Garching (and perhaps Chile) needs a new testbench. To be operated by the FIERA controller, the testbench will utilise the knowledge gained from the many years of experience with the present CCD testbench.

We are also developing an optical set-up to scan a 2 micron wide (minimal wings) spot of variable wavelength across the pixels of CCD devices. We will use this apparatus to measure the diffusion of photoelectrons that causes degradation of PSF in CCD devices. PSF degradation was an unwelcome surprise during the CES upgrade and we must become expert at measuring this behaviour for all of our CCD chips. High quality PSF is important for nearly every application, but especially so for adaptive optics and high-resolution spectroscopy.

12. Optical Detector Workshop – October 8-10, 1996

The ESO CCD workshops held in 1991 and 1993 were valuable venues of information exchange about astronomical CCD detectors. After a brief respite, ESO will continue the series with an Optical Detector Workshop to be held during October 8–10, 1996 in Garching. The attendance of the workshop is being limited due to space constraints and our desire to create an intimate setting for information exchange. We have received confirmations of attendance from most of the leading manufacturers and major observatories. (If you wish to attend, please submit a request to jbeletic@eso.org)

13. Closing Comments

The optical detector team has established a coherent plan of activities for improving ESO's technology in this critical area. Our mission is to develop, implement and maintain optical detector systems that are the best that science and technology can provide. We encourage feedback on the direction and plans that we present in this report.

(Please send comments to: jbeletic@eso.org or odteam@eso.org)

Pointing and Tracking the NTT with the "VLT Control System"

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Introduction

One of the three main goals of the NTT Upgrade Project is to test the VLT control system in real operation before installation on Paranal. Although NTT and VLT have large differences in optics, mechanics and electronics, the VLT Common Software and the standardisation of VLT control electronics provide a common base. The strategy of the NTT Team has been to develop NTT unique