

Review of AO Wavefront Sensing Detectors

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ABSTRACT

The detector is a critical component of any Adaptive Optics WaveFront Sensing (AO WFS) system. This paper examines the roadmap of detectors used for AO Wavefront Sensing by reviewing; detectors used in past instruments, detectors that are available now and will be used in future instruments on existing telescopes, and the requirements and status of new detectors whose development is critical for the success of the next generation of extremely large telescopes (E-ELT, GMT, and TMT). In doing so, the paper will also report on the AO WFS detectors currently under test at ESO.

The required performance combination of fast frame rate, high quantum efficiency, low read noise and dark signal, number and size (24-50 μm) of pixels pushes detector technology to the edge such that in many cases custom detector developments are required.

Keywords: Adaptive Optics Detector, AO Wavefront Detector, Wavefront Sensor, L3Vision CCD, CMOS Imager, SPADA, Polar Co-ordinate CCD, pnCCD, Speedster.

1. INTRODUCTION

The performance of the wavefront sensor (WFS) detector in the past has always been a very important consideration when designing an Adaptive Optics (AO) WFS system. In most cases, this has led to a custom development to build a detector with very demanding requirements of high quantum efficiency (QE) and very low read noise (RON) and dark current at fast frame rates. For the success of the next generation of extremely large telescopes (E-ELT, GMT, and TMT), the requirements of high QE and low RON at fast frame rates remain critical, however, one has the added demand of larger format size.

AO WFS systems may be categorized in the following way:

1. **Type of guide star:** natural guide star (NGS) or artificial laser guide star (LGS). LGSs are created by launching lasers into the sky to either excite atoms in the mesospheric (at altitude of $\sim 90\text{km}$) sodium layer (Sodium LGS) or using Rayleigh backscatter from molecules and particles located in the low stratosphere at altitude of 10-30km (Rayleigh LGS). Sodium LGS and Rayleigh LGS have single detection wavelengths of 589nm and 532nm (typically) respectively, while optical NGS have typically detection wavelength range of 400-950nm, and infrared (IR) NGS have wavelength range of 1.0-2.2 μm . The type of laser system can be further divided into continuous wave (CW) or pulsed.
2. **Type of WFS sampling technique:** Shack Hartmann (SH), curvature or pyramid.
3. **Spatial sampling:** The order of the correction (= number of sub-apertures) spans from low order (2x2) systems used primarily with NGS for tip/tilt correction to high order wave front correction systems using LGS or NGS. Systems currently in use (e.g. VLT NAOS SH WFS and MACAO curvature WFS) have 60 sub-apertures. Systems in development (VLT AOF – MUSE and HAWK-I and SPHERE) require 1600 (40x40) sub-apertures. Future systems for the ELTs are proposed to have 60x60 to 120x120 (TMT), 84x84 to 126x126 (E-ELT) or higher, 256x256, for NGS extreme AO (XAO). The number of pixels per sub-aperture vary from a single pixel for curvature WFS, to 2x2 for Quad SH and pyramid WFS, to 6x6 for the VLT AOF and SPHERE SH WFS, to 20x20 for the proposed E-ELT SH LGS WFS to sample the spot elongation.
4. **Temporal sampling** (i.e. the frequency of the WFS AO servo loop): As low as 25Hz for tip-tilt NGS and “truth” wavefront sensors to 500Hz in current AO systems, 1200Hz in systems under development, and up to 3kHz for Extreme AO (XAO) on ELTs.

5. A **myriad of different proposed implementations** optimized for a particular set of science objectives: Single-Conjugate AO (SCAO), (Laser Assisted) Multi-Conjugate AO (LA-MCAO), XAO, (Laser Assisted) Multi-Object AO (LA-MOAO), (Laser Assisted) Ground Layer AO (LA-GLAO), Laser Tomography AO (LTAO), etc. etc.

It is difficult to conceive a single detector that will meet the needs of this diverse range of applications; i.e. operate optimally with high QE in both the optical and IR wavelength ranges (0.4-2.2 μm), maintain low noise (RON and dark current/counts) over a wide range of frame rates from 25Hz to 3kHz, and provide enough pixels to spatially sample the wavefront from 2x2 sub-apertures for simple tip-tilt correction up to 256x256 for XAO. For these reasons, a wide range of AO detectors have been proposed and manufactured.

Detector engineers and scientists have employed many different technologies in their pursuit to develop the ideal detector for AO:

- 1) CCDs that are read out through multiple outputs to achieve high frame rates while maintaining low read noise,
- 2) Electron Multiplying CCDs (EMCCD) that have special gain stages in their serial registers that accelerate the electrons through high potential fields so that by impact ionization amplify the signal in the charge domain. EMCCDs achieve sub-electron read noise at pixel rates up to 25 Mpix/sec per output,
- 3) CCDs (CCID-35^[4] and Polar Co-ordinate^[24] CCD) that have architectures custom designed to a particular AO application, and
- 4) Single Avalanche Photodiodes (APD) and Single Photon Avalanche Diode Arrays (SPADA)^{[26][27]} that operate at very high gains to discriminate and count single photon events and thus essentially offer zero read noise.

This paper will describe: 1) the different detectors that have been manufactured up to date, 2) the new ones in fabrication (e2v CCD220^{[10][11][12]}, MPI-HLL⁴ pnCCD^[19], and CCID-56^[3]) that are required to meet the current needs of instruments, and 3) the requirements and status of new detectors whose development are critical for the success of the next generation of extremely large telescopes (E-ELT, GMT, and TMT). As most developments have been in the optical wavelengths, a separate section is dedicated to the recent advances made in IR AO WFS detectors

2. PAST DETECTORS

Table 1 contains a list of optical AO WFS detectors that have been designed and built over the past 10-15 years. The major past developments have been designed and fabricated by MIT/LL¹ and e2v technologies and have mostly involved designs based on CCDs that achieve high frames and low read noise by reading out through multiple amplifiers. Multiple amplifiers keep the pixel rates slow enough to filter out (bandwidth limit) the RON. Split frame transfer CCDs, MIT/LL CCID-26^[1], e2v² CCD39, and e2v² CCD50 (Table 1), of array sizes up to 128x128 and read out noise of 5-7 e⁻ at 1,000 fps (frames per second) have been used extensively.

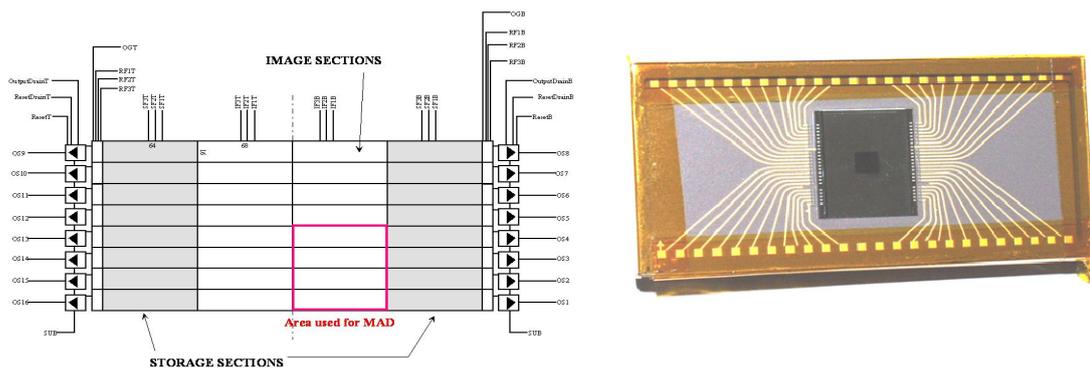


Figure 1: The CCD50: An example of a multi-output split frame transfer CCD. Left: Chip layout; 16 output amplifiers are used to achieve low read noise at 1 kfps. Right: Photo of CCD50

¹ MIT/LL - MIT Lincoln Laboratory, <http://www.ll.mit.edu>

One way to break the trade between read out speed and noise is to custom design the CCD architecture to the AO application, as was done with the CCID-35^[2]. The CCID-35 was conceived by James Beletic and Reinhold Dorn (ESO) and designed and fabricated by Barry Burke of MIT Lincoln Laboratory. It was designed to replace expensive (US\$2k per APD) and fragile arrays of single APDs used in AO curvature WFS systems of the ESO VLT Interferometer. The architecture best suited to this application required, 1) > 60 extremely large (360 μ m) square pixels (larger than at the time thought possible in a single pixel) to ease the attachment of fibers, 2) two storage regions per pixel to save the accumulating charge from the intrafocal and extrafocal positions, and 3) the ability to store and read out the previous image while integrating on the next image.

The resulting design (Figure 2: Design of the MIT/LL CCID-35. A group (b) of 10 sub-apertures (a) feed into a single serial register which is repeated 8 times (c) for a total of 80 sub-apertures) of the CCID-35 consisted of 8 groups of 10 sub-apertures. Each group of sub-apertures is read out at slow speed (50kpixel/sec) through a serial register and amplifier (for a total of 8 amplifiers). Each sub-aperture consists of an array (superpixel) of 20x20 18 μ m pixels. The storage registers at each end of the superpixels accumulate photons noiselessly in the charge domain at > 2 kHz from intrafocal and extrafocal positions. An additional storage buffer per pixel holds the current image while a new one is accumulated.

Table 1. List of optical AO WFS Detectors that have been designed and built over the past 10-15 years.

| Manufacturer | MIT/LL ¹ | MIT/LL ¹ | MIT/LL ¹ | MIT/LL ¹ | e2v ² | e2v ² | e2v ² | e2v ² | PoliMI ³ | MPI-HLL ⁴ |
|---|---------------------------------|---------------------------------|-----------------------------------|--|---|---------------------------------|---|-----------------------------------|---------------------|------------------------------------|
| Type Number | CCID-26/64 | CCID-26/128 (CCID-18) | CCID-35 | CCID-56B/D | CCD39 | CCD50 | CCD60 | CCD220 | SPADA | pnCCD |
| Architecture | Split Frame Transfer | Split Frame Transfer | custom | Split Frame Transfer | Split Frame Transfer | Split Frame Transfer | Frame Transfer | Split Frame Transfer | custom | Split Frame Transfer |
| Pixel size (μ m) | 21 | 21 | 360 | 21 | 24 | 24 | 24 | 24 | 50 | 51 |
| Image Array Format (pixels) | 64*64 | 128*128 | 10*8 superpixels | 160*160 | 80*80 | 128*128 | 128*128 | 240*240 | 60 circular array | 264*264 |
| Frame Rate (fps) | 600 | 10,000 | 4000 | 800 | 1000 | 1000 | 1000 | 1500 | 20,000 | 1000 |
| Number of Outputs | 4 | 16 | 8 | 20 | 4 | 16 | 1 | 8 | 60 | 8 (528) ⁵ |
| Read Noise (e- rms) | 6-7 | 4.5 at 1kfps 10 at 10kfps | 1.5 | 2.4 | 10 | 5 | << 1 16Mpix/sec | << 1 16Mpix/sec | << 1 | 2.4 |
| Excess Noise | None | None | None | None | None | None | 1.4 (L3Vision) | 1.4 (L3Vision) | None | None |
| Thickness, Silicon Material, and Technology | 20 μ m Standard Silicon CCD | 20 μ m Standard Silicon CCD | 40 μ m HiRes ⁶ CCD | 40 μ m HiRes ⁶ CCD (B) 75 μ m HiRes ⁶ , substrate bias ⁷ CCD (D) | 20 μ m Standard Silicon CCD | 20 μ m Standard Silicon CCD | 13 μ m thick Standard Silicon EMCCD | 13 μ m Standard Silicon EMCCD | APD | 450 μ m HiRes ⁶ CCD |
| QE | ~ 90% | ~ 90% | ~ 90% | ~ 90% | ~ 90% | ~ 90% | ~ 90% | ~ 90% | ~ 30-40% | ~ 90% |
| Special Features | | Integrated Shutter | Custom architecture | Low noise JFET | Optional Peltier | | L3Vision, Optional Peltier | L3Vision, Peltier | Photon counter | Amplifier per column |
| Facility (incomplete) | KECK | | ESO MACAO, CFHT Flyeyes | KECK | LBT, NAOMI, ESO MAD, Gemini ALTAIR, MMT, Palomar. | ESO NAOS, Palomar AO | NAOMI-William Herschel, LBT, ESO HOT | ESO AOF & SPHERE | ESO MACAO | LBT |

2 e2v – e2v technologies, <http://www.e2v.com>

3 PoliMI - Politecnico di Milano, <http://www.dei.polimi.it>

4 MPI-HLL – Max Planck Institut Halbleiterlabor, <http://www.hll.mpg.de>

5 pnCCD has column parallel read out for a total of 528 amplifiers. However, the pnCCD has an on-package read out IC (called CAMEX) that multiplexes the video down to 8 outputs.

6 HiRes – High Resistivity silicon for deep depletion and higher QE in the far red.

7 'Substrate bias' is added to generate deeper electric fields to improve pixel cross-talk in devices made from thicker silicon. Thicker silicon provide higher QE in the far red.

Dorn^[4] as part of his Ph.D. thesis demonstrated read out noise as low as $1.5e^-$ rms at 4 kfps, $QE > 80\%$, and dark current of $< 0.25e^-$ /pixel at 50 fps at 197K. Dorn concludes that the CCID-35 is a real alternative to arrays of single APDs. The CCID-35 has been successfully used (April 2007) in FlyEyes^[5] by the CFHT as the sensor to upgrade their 19 element PUEO AO system to an 80 element "PUEO NUI" system.

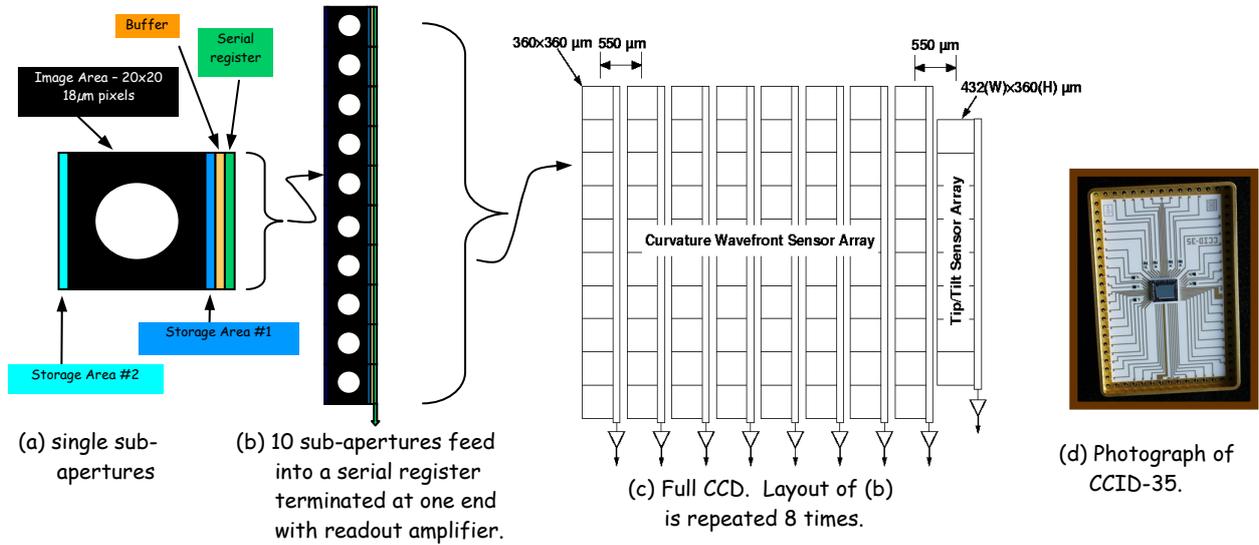


Figure 2: Design of the MIT/LL CCID-35. A group (b) of 10 sub-apertures (a) feed into a single serial register which is repeated 8 times (c) for a total of 80 sub-apertures

Another way to break the speed versus noise trade is to improve the output amplifiers by optimizing better the geometry of the amplifier, oxide thicknesses, or type of amplifier. Barry Burke (MIT/LL) has designed a new p channel JFET amplifier for the 160×160 $21 \mu\text{m}$ pixel CCID-56^[3]. The effective noise of JFET amplifiers is much less than conventional MOSFETs because JFETs have 1) lower noise spectral voltage, approximate half that of MOSFETs (Figure 3), and 2) higher responsivity ($30 \mu\text{V}/e^-$ versus $20 \mu\text{V}/e^-$) due to the lower sense node capacitance of JFETs. Burke is reporting^[13] low read noise of $2.4e^-$ at pixel rates of 1 Mpix/sec (800fps), but believes to be limited by the MIT/LL controller electronics and not the fundamental noise limit of the device. Further results by other groups will be available soon.

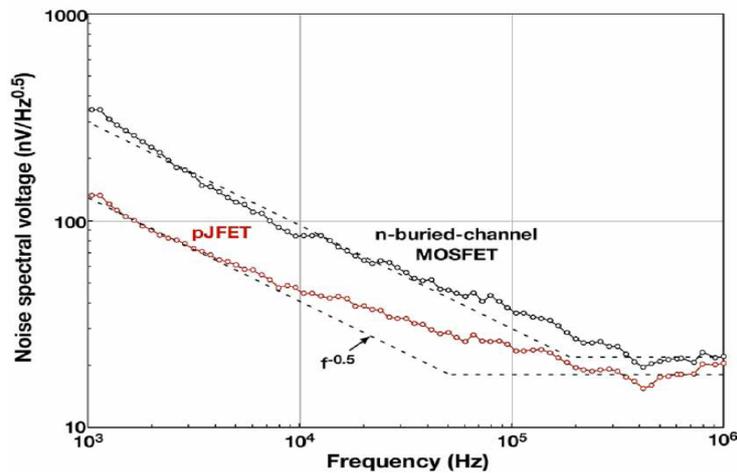


Figure 3: Comparison of noise spectral voltage of JFET and MOSFET amplifiers. Figure courtesy of MIT/LL^[13].

In 2001, e2v introduced their L3Vision^[14] EMCCDs. EMCCD is a CCD that has a multi-stage (> 500) gain register between the CCD shift register and the output amplifier. Each gain stage achieves a small probability ($\sim 2\%$) of electron multiplication by impact ionization in a similar way to an avalanche diode. By having a large number of gain stages gains in excess of 1000 are possible, thus, enabling L3Vision outputs to achieve effective sub-electron read noise at pixel rates up to 25 Mpixel/sec. The e2v 128x128 24 μm pixel CCD60 achieves sub-electron read noise at 1,000 fps with a single output.

Another custom detector is the PoliMI SPADA^[6] monolithic array of APDs developed for AO curvature WFS on the ESO VLT Interferometer. 60 SPAD elements are arranged in a circular concentric geometry, such that the unit is a plug in replacement for the existing array of single APDs. The APDs operate at very high gain in Geiger mode to discriminate and count single photon events. Active quench and reset circuit are provided on separate custom monolithic circuits. QE of $> 40\%$, dark count rates of < 3000 counts/sec/pixel, and essentially zero read noise at frame rates up to 20 kfps are reported.

For pulsed LGS applications, it is advantageous to have a fast ($< 1\mu\text{s}$ open/close time) shutter: 1) to range gate to within a few km the return light from a pulsed laser and thus dramatically reduce the spot elongation (see section 4 for explanation), 2) to shutter out fratricidal images from neighboring lasers in a multi-laser system and the Raleigh backscatter from the lower parts of the atmosphere. This fast shuttering is not possible by opto-mechanical means. One solution is to build an integral electronic shutter directly into the detector.

Bob Reich and colleagues at MIT/LL^[7] have pioneered such a technique by implanting a “p” layer below the buried channel and an n^+ region (shutter drain) under the channel stop. Left of Figure 4 shows the resulting pixel cross section (a) and the depletion regions for the shutter open (c) and closed (d) conditions. Shutter times (b) of 10 ns and extinction ratio (ratio of signal detected shutter opened to shutter closed) of 10^4 for wavelengths below 540 nm have been demonstrated. This integral electronic shutter has been built into the CCID-26/128^[1]. e2v has also built a similar technology integral electronic shutter into the CCD220 (code named CCD219) for demonstration purposes.

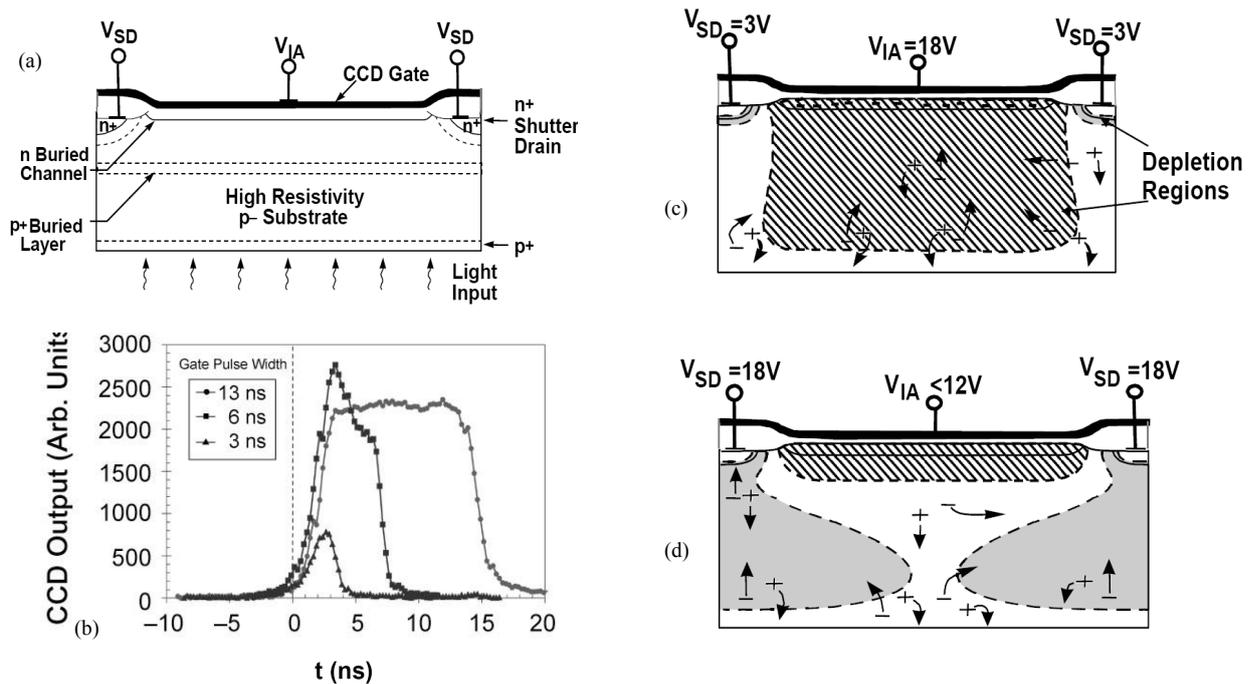


Figure 4: Left: Cross section of pixel, perpendicular to charge transfer, with the electronic shutter structure showing (a) the location of shutter drain and added “p” implant below the buried channel and depletion regions for (b) shutter opened and (c) shutter closed conditions. Right: CCD response versus time t , for imaging-array-gate pulse widths of 3 ns, 6 ns and 13 ns illustrating transient response of the detector shutter. Figure courtesy of MIT/LL [7].

3. DETECTORS FOR CURRENT INSTRUMENTS AT ESO

ESO is involved in the advanced stage of developing/testing two detectors: the e2v CCD220 and the MPI-HLL pnCCD.

e2v CCD220:

ESO and JRA2 “Fast Detectors for Adaptive Optics” FP6^{[8][9]} OPTICON⁸ network funded e2v to develop a compact Peltier cooled sensor, the CCD220, to meet the requirements of WFS for the next generation of VLT instruments (SPHERE, AOF – MUSE and HAWK-I).

The CCD220^{[10][11][12]} (schematic left in Figure 5) is a 24 μm square 240x240 pixels split frame transfer back illuminated L3Vision CCD. The image and store area (store is optically shielded) are built with 2-phase metal-butressed parallel clock structures to enable fast line shifts in excess of 7 Mlines/s for total transfer time from image to store of 18 μs and low smearing of under 2% at 1,200 fps. Eight electron-multiplying gain L3Vision^[14] registers operating at greater than 13 Mpixel/sec enable sub electron noise to be achieved at frame rates of 1,500 fps. With an output amplifier read noise of 70e- at unity gain, an electron-multiplying gain of 700 enables an overall effective read noise of under 0.1 e- (70 e-RON/700 of gain register) can be achieved.

The CCD220 is encapsulated in a 64 pin package (right in Figure 5) with a custom-designed integral thermo-electric cooler that has been verified^{[10][15][16]} to cool the CCD below -45°C to achieve the required < 0.01 e-/pix/frame total dark current. The package is sealed and back-filled with 0.9 bar of Krypton gas to minimize heat transfer to the outside.

As part of JRA2, a consortium of French institutions^[17] LAOG-LAM-OHP⁹, have developed a low noise state of the art controller, called OCam^[16] (photo left Figure 6); one of which is on loan to e2v for testing the production of CCD220s. Image in the right of Figure 6 was taken by the OCam camera with an engineering CCD220 cold and with L3Vision multiplication gain. With a normal camera at same exposure time, this image was completely black. Using OCam as their test camera, e2v have delivered several standard silicon and the more speculative Deep Depletion CCD220 to ESO that meet specifications. The Deep Depletion devices enable much higher QE in the “red”. Further evaluation of the technology is underway at ESO.

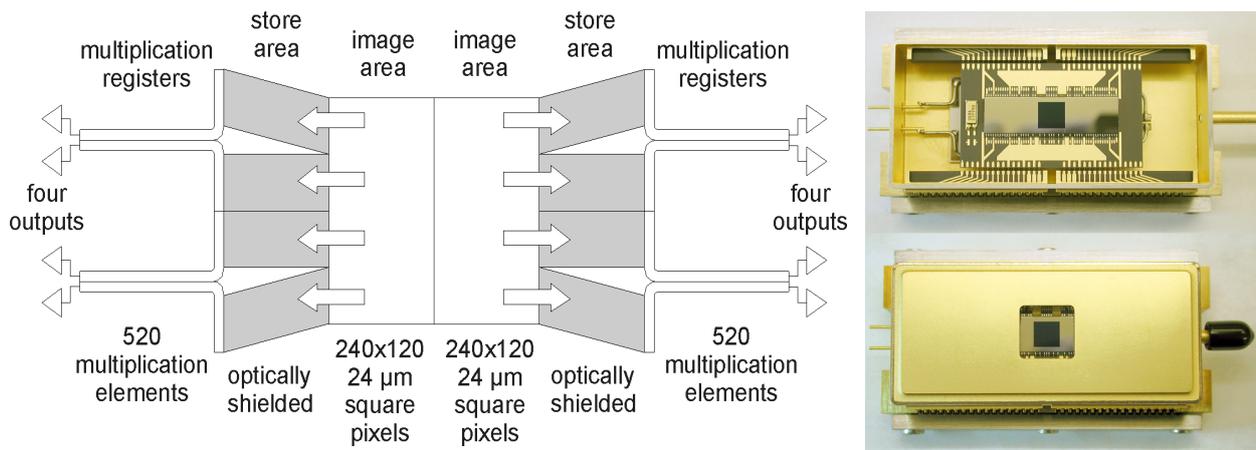


Figure 5: Left: Schematic of e2v 240x240 pixel L3Vision CCD220. Eight electron-multiplying (gain) registers enable sub electron noise at frame rates of 1500 fps. Right: Photograph of CCD220 package. The package contains an integral Peltier that has been verified to cool the CCD below -45°C to achieve < 0.01 e-/pix/frame total dark current

8 The Optical Infrared Co-ordination Network for Astronomy (OPTICON) comprises 47 international contractors working together towards further integration of European astronomy. OPTICON is funded by the European Commissions 6th Framework program under contract number RII3-Ct-2004-001566.

9 LAOG-LAM-OHP, Laboratoire d'Astrophysique de l'Observatoire de Grenoble, Laboratoire d'Astrophysique de Marseille, and Observatoire de Haute Provence.



Figure 6: Left: Close-up photo of the OCam camera. Sub-electron noise has been demonstrated. Right: Image of OCam team (Left to right: Christian Guillaume, Jean-Luc GACH, Philippe Feautrier, and Philippe Balard) taken by the OCam camera with CCD220 cold and with L3Vision multiplication gain

For the scheduled deployment of the CCD220 on VLT instruments, ESO are at an advanced stage of developing an AO version of the New General detector Controller^[18] (AONGC). The AONGC will re-use much of the front-end analogue design developed by the Ocam team (Philippe Balard, Philippe Feautrier, Jean-Luc GACH, Christian Guillaume, and Eric Stadler).

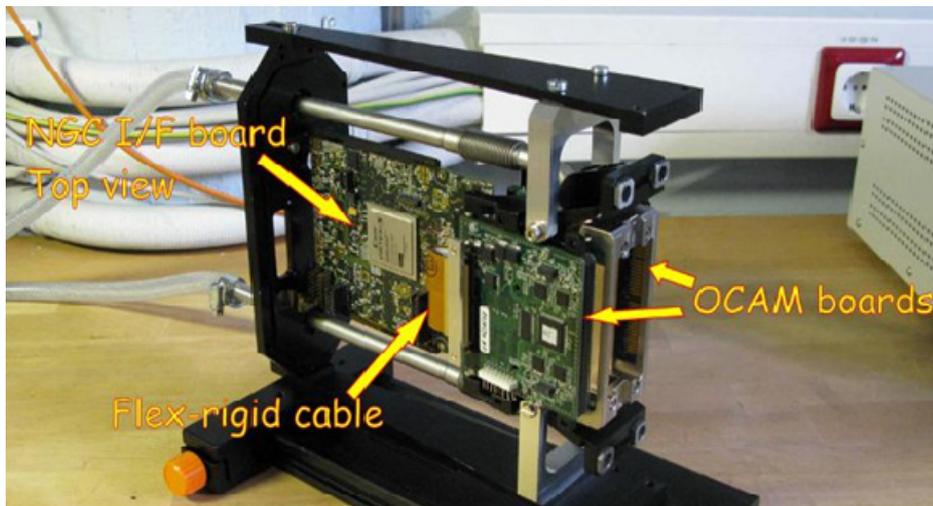


Figure 7: Photograph of the NGC AO WFS Camera under development at ESO. Much of the technology developed for OCam will be re-used in NGC.

MPI-HLL pnCCD:

The second detector ESO is testing (funding for testing provided by FP6 OPTICON⁸) is the 51 μ m 264x264 pixel pnCCD^[19] (photo right Figure 8) developed by MPI-HLL. The device was developed for particle physics and X-ray astronomy. With low read noise (2.4e rms) at fast frame rates (1000 frames/s) and high QE in the “red”, is of interest as a

NGS AO detector. MPI-HLL specializes in detectors with large pixel pitch (36-300 μm), thick (300-500 μm) but fully depleted, and non-overlapping Aluminum clocks that have very low RC time constants ($\sim \text{ns}$) enabling high speed operation.

The read out architecture of the pnCCD (left Figure 8) of split frame transfer and amplifier per half column (for 528 amplifiers total) enables low read noise at fast frame rates. Four read out integrated circuits, ROICs, (called CAMEX) wire bonded to the pnCCD amplifiers provide analog multi-correlation double sampling (CDS) processing and output multiplexing to reduce the number of video outputs per CCD to 8, thus simplifying the back end support electronics.

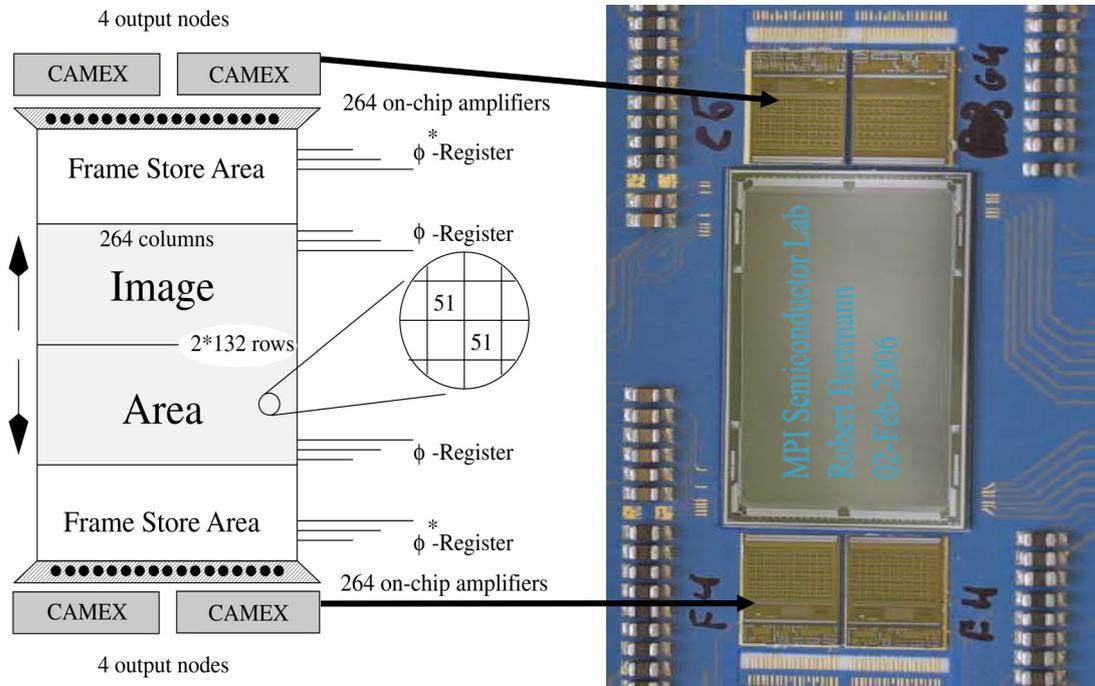


Figure 8: Schematics (left) and photograph (right) of the 51 μm 264x264 pixel pnCCD (courtesy of [17]).

The device tested at ESO was cosmetically clean with no observable hot or dark pixels at frame rates down to 25 fps and operating temperature of -45°C . The gains of amplifiers and CAMEX were uniform (Figure 9) with 99% of pixels varying by $< 3.5\%$ (0.8% rms).

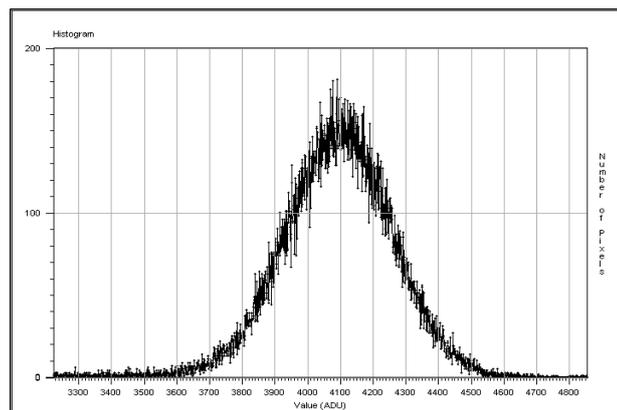


Figure 9: Histogram of a flat field image measured at ESO demonstrates good gain uniformity of amplifiers and CAMEXs (99% of pixels vary by $< 3.5\%$).

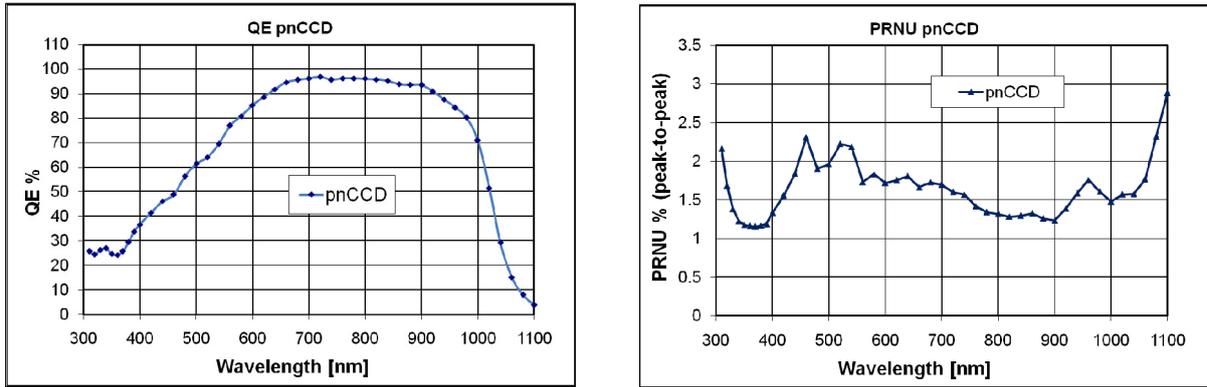


Figure 10: Left: Measured QE of the pnCCD showing excellent “red” response. Right: Measured PRNU (% peak-to-peak) versus wavelength at bandwidth of 7nm demonstrating low fringing (Both QE and PRNU were measured at ESO by M. Downing).

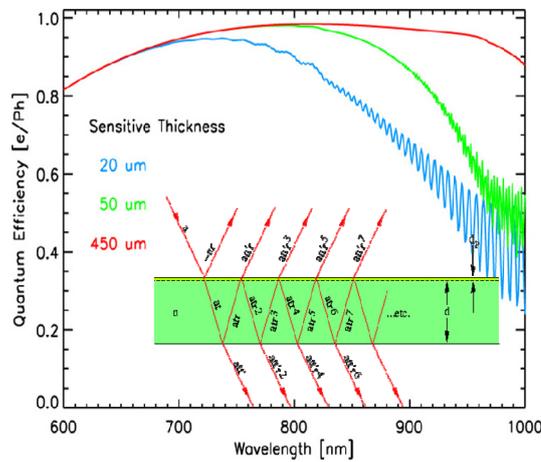


Figure 11: Theoretical analysis of fringing for various thicknesses (20, 40, and 450 μm) of silicon. The plot demonstrates why the pnCCD manufactured from 450 μm thick fully sensitive silicon has extremely low fringing (diagram courtesy of MPI-HLL).

High QE in the “red” is possible, as the device is built from 450 μm thick (fully sensitive) silicon. QE measured at ESO (Figure 10) demonstrated QE > 80% from 560nm to an impressive 980nm. The measured Photon Response Non-Uniformity, PRNU, (Figure 10) shows very good uniformity even at long wavelengths. Extremely low fringing is observed as theoretical analysis predicts (Figure 11). The increase in PRNU longwards of 1000nm is due to a decrease in QE sensitivity at the edges of the device and not fringing. The measurements (Figure 12) of the pixel point spread function, PSF, (for measurement technique see [21]) and the plot of the spot scan across the pixel show excellent spatial performance demonstrating full sensitivity (full depletion) through the whole silicon thickness.

With recent improvements of active reset of the read out node and increased bandwidth in the CAMEX, low read noise of $\sim 2e^-$ at 950fps has been demonstrated.

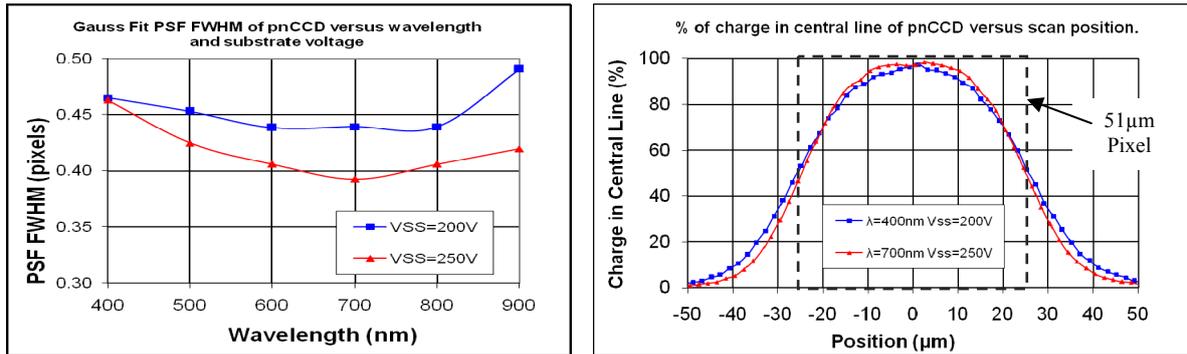


Figure 12: Left: Measured PSF (FWHM) versus wavelength and substrate voltages of 200 and 250V. Right: Percentage of charge collected in a pixel as a $2\mu\text{m}$ spot is scanned across at 400nm and 700nm and substrate voltages of 200V and 250V. In the plot the middle of a pixel is located at $0\mu\text{m}$ (Data measured at ESO).

MPI-HLL are also developing (partially funded by ESO and FP6 OPTICON⁸) an APD version of the pnCCD called the AVACCD^[20]. The AVACCD operates in Geiger-mode. The status to date is that key components have been successfully tested and qualified including the demonstration of a working single avalanche cell. Various test AVACCDs (example Figure 12) with different pixel geometries and process variations have been fabricated and are currently under test. Important results on gain, avalanche probability, and avalanche cross-talk are due early 2010.

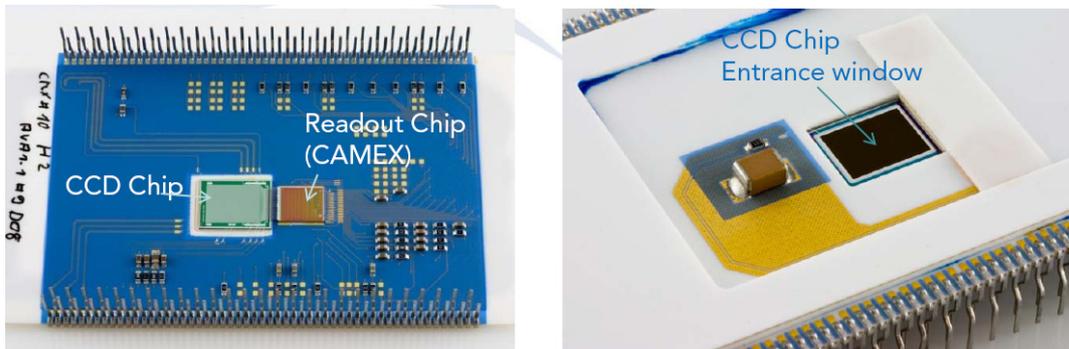


Figure 13: First avalanche pnCCD ($51\mu\text{m} \times 51\mu\text{m}$ 132 x 176 pixels) under test (photographs courtesy of Ivan Ordavo of MPI HLL).

4. THE FUTURE: THE ELT CHALLENGE

For WFS on the E-ELT, four different types of applications (Figure 14) for detectors have been identified:

- 1) $< 256 \times 256$ pixels detector for low order AO, Shack Hartmann Quad-Cell, Pyramid, Tip-Tilt sensors, Guiding applications where an existing optical high performance detector such as the CCD220 or pnCCD is sufficient,
- 2) Large LGS/NGS SH WFS optical detector with very large pixel format to sample the spot elongation, fast frame rate (700 fps), high QE ($> 90\%$), and low noise ($< 3e^-$),
- 3) XAO NGS pyramid WFS optical detector with a much smaller number of pixels ($\sim 256 \times 256$), but read out at extremely fast frame rate (3 to 4 kfps), ultra low read noise/dark current ($< 1 e^-/\text{pixel}/\text{frame}$), and high QE $> 90\%$ especially in the "red" (450-900nm),
- 4) WFS and Tip-Tilt InfraRed (IR) detector.

The first one can be met by existing detectors. The IR detector will be discussed in the next section. The requirements of the large LGS/NGS and the XAO detectors differ sufficiently to believe that separate developments are required. The

large LGS/NGS detector is thought to be the most critical for the success of the E-ELT thus is the one so far concentrated upon.

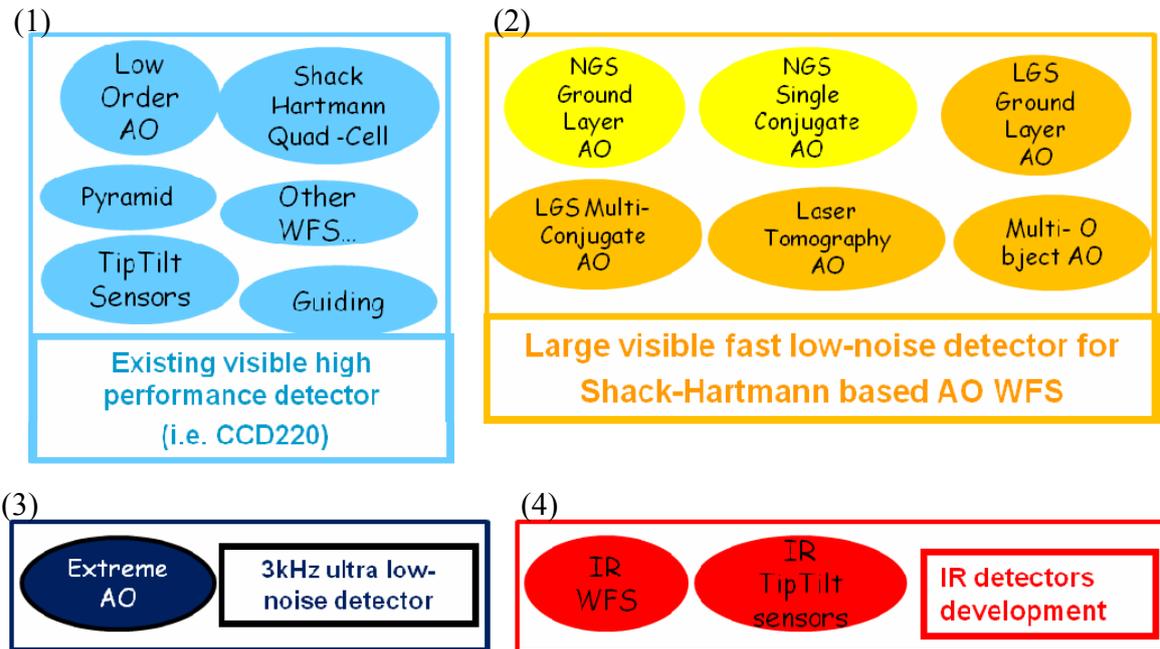


Figure 14: Diagram showing the breakdown, into four different application areas, of detectors for WFS on the E-ELT.

Spot elongation of LGS (Figure 15) is considered one of the major challenges of AO WFS systems of ELTs. The spot elongation is due to the finite thickness of the sodium layer and the offset between the laser projection point and the sub-apertures of a SH WFS. The elongation or spreading of the LGS image results in a decrease in the signal to noise ratio (SNR) resulting in an increase of the centroid error, and subsequently increased error of the wavefront phase reconstruction.

The current LGS WFS system for the E-ELT (an AO Telescope) baselines the following: 1) up to 6 CW¹⁰ Sodium LGSs projected from the sides of the telescope, 2) enough laser power to provide 1000 photons per sub-aperture, 3) high spatial sampling of 84 x 84 sub-apertures (goal 126 x 126) with 20 x 20 pixels per sub-aperture to adequately sample the spot elongation, and 4) high temporal sampling of 700 Hz.

From the top level science requirements, the following requirements for the large LGS/NGS AO WFS detector have been justified:

- 1) Minimum format size of 1680x1680 pixels,
- 2) Big pixels of 20-28µm, to ease the optical system design (mechanical alignment and stability), but small enough to avoid excessive dark current/counts, charge transfer inefficiency (CTI), or manufacturability problems,
- 3) Versatility of 100% fill factor for maximum flexibility; at least within the sub-aperture and if possible over the whole array (to make it possible to decide later to change laser projection site and/or mix of sub-apertures/pixels),
- 4) Low dark current and read noise such that total noise is $< 3e^-$ rms.
- 5) High QE over wavelength of 450-950nm and especially at 589 nm (LGS wavelength),

¹⁰ CW = Continuous Wave

- 6) Equivalent exposure time of frame rates from 100fps to 700 fps.
- 7) Low read out latency (< 7% of exposure time) so that corrections can be applied as quick as possible after the exposure ends,
- 8) Detection signal limit of 4000e-/pixel; laser power will be limited so the system will be photon starved (expect only 1000 photons per sub-aperture per frame),
- 9) Good spatial characteristics, PSF < 0.8 pixel FWHM¹¹, to accurately determine where the photons arrived,
- 10) As cosmetically defect-free as possible (< 0.1% of defective pixel),
- 11) Ease of use/compact size: integrated read-out electronics (CDS and ADC) if possible, simple (if possible digital) industry standard interface (e.g. LVDS¹² ANSI/TIA/EIA-644, JESD204A¹³, or RocketIO¹⁴). Integral Peltier cooled package for compact size, maintenance free, and minimal support equipment.

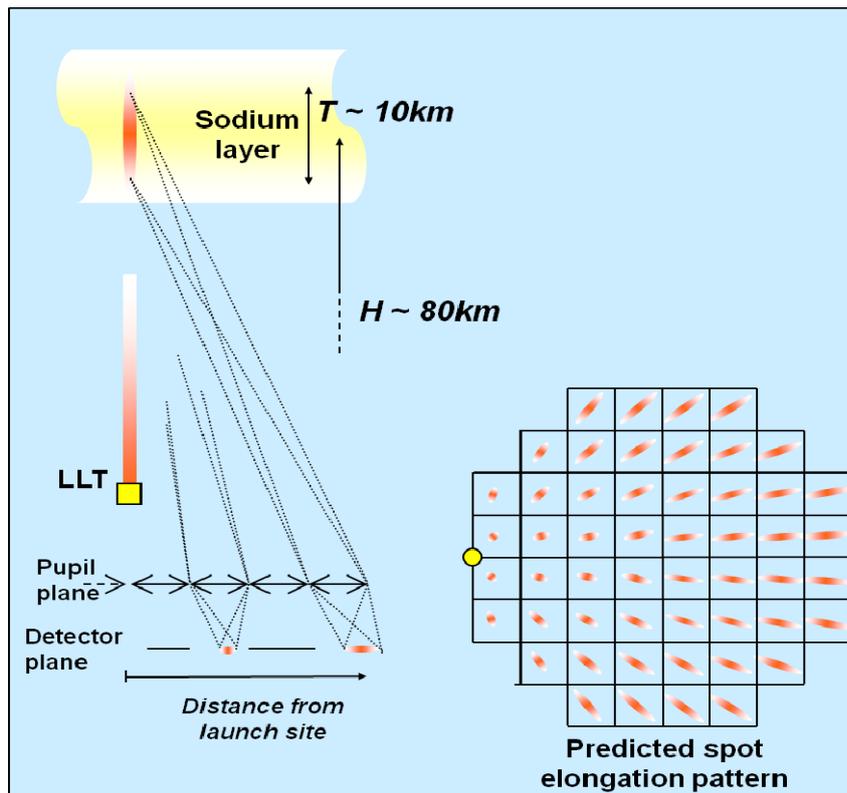


Figure 15: The spot elongation is due to the finite thickness of the sodium layer (10-15km) and the offset between the laser projection point and the sub-apertures of SH WFS. The LGS baseline design is to have the lasers projected from the telescope sides

The development plan for the large LGS/NGS AO WFS detector is a multi-phased (a progressive risk retirement) development over ~ 9 year duration (Figure 16) to have detectors available on time for the NGS first light AO systems of the E-ELT.

¹¹ FWHM = Full Width Half Maximum

¹² LVDS = Low Voltage Differential Signal

¹³ www.jedec.org/download/search/JESD204A.pdf

¹⁴ http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex4/capabilities/rocketio.htm

As part of the ELT design study (DS) program¹⁵, a number of detector design studies were performed by industry during 2007. The studies showed that conventional CCD arrays, mosaics of CCDs or pnCCDs, and CCDs or silicon photodiodes (e.g. Teledyne HyViSI) bump bonded to CMOS read out structures: 1) will unlikely meet either the low read noise requirements and/or require cooling below 70K, or 2) suffer from serious trade-offs between power dissipation, noise, latency and read out speed, and/or from manufacturability issues. Other solutions such as 3-D integrated Focal Plane Array^[13] (e.g. MIT/LL) were considered technologically immature.

The design studies identified four possible technologies^[28]:

- 1) Back-Side Illuminated (BSI) CMOS Image Sensor (CIS),
- 2) Front-Side Illuminated (FSI) CMOS Imager with advanced gapless microlenses,
- 3) APDs in linear or Geiger mode (SPADA – Single Photon Avalanche Diode Array),
- 4) Orthogonal Transfer WFS Electron Multiplying CCDs (OT WFS EMCCD).

A fifth possibility is the polar coordinate CCD^{[23][24]} which was initially conceived by Sean Adkins, James Beletic, Barry Burke and Jerry Nelson, and is being developed by Sean Adkins of KECK in collaboration with MIT/LL (Brian Aull, Brad Felton and Robert Reich) to be used with both CW and pulsed lasers.

During 2008 and 2009, BSI CMOS Imager (judged most likely to succeed) technology (pixel) demonstrators were built and tested (as part of the ELT DS) to assess and validate various CMOS technologies, their capability to meet critical requirements (especially of image lag, read noise, and speed), and scalability to full-size devices.

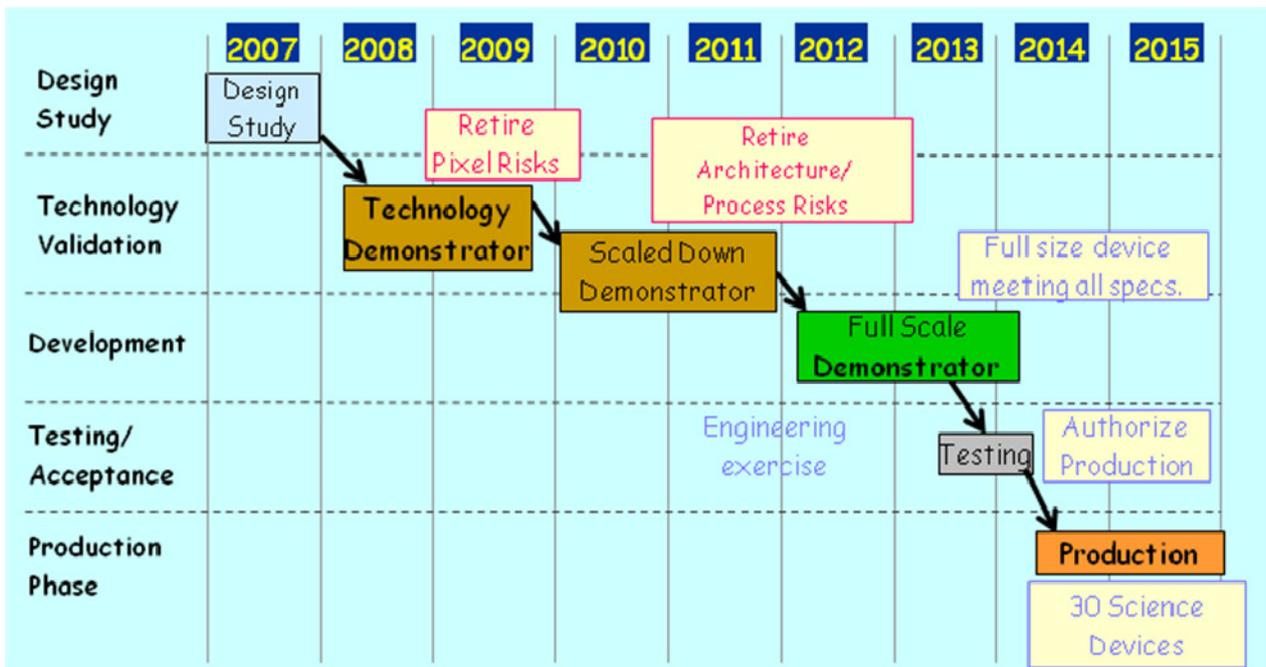


Figure 16: The multi-phase development plan of the large optical NGS/LGS WFS detector showing how risk is progressively retired; Design Study to investigate possible technologies, Technology Demonstrator to retire pixel risks, Scaled Down Demonstrator to retire architectural and process risks, and finally, the full scale development which should be mostly an engineering exercise and production run to manufacture 30-50 devices.

The next phase, in 2010 and 2011, is to build and test Scaled Down Demonstrators (SDD) to retire architecture and process risks. The SDD will be large enough (~ ¼ size) to be used as a detector for first light NGS AO WFS systems on

¹⁵ The ELT DS is a technology development program towards the E-ELT sponsored by the European Commission within the Framework Program 6 (FP6)

the E-ELT. The SDD will be followed by the full scale development (mainly an engineering exercise) and production run of 30-50 devices.

Back-side Illuminated (BSI) CMOS Imager:

Recent developments in CMOS imagers have produced rapid improvement in performance where read out noise of 2-3 e-, dark current as low as 10 pA/cm² at room temperature and QE > 80% have been demonstrated in several prototype detectors^{[29][30][31][32][33]}. This type of performance now rivals CCDs. One of the main drivers behind the rapid development has been the market of mobile phone with integrated photo camera where it has been projected¹⁶ that as the pixel size shrinks below 2 μm, CMOS imagers will become substantially cheaper than CCDs for the same overall performance.

The rapid progress has come about through several innovative improvements:

The **first** is the Pinned Photo Diode (PPD) that capitalizes on the same phenomenon, Multi Pinned Phase (MPP) that enables the lowest dark current in CCDs. In both cases a high concentration of holes is created at the surface which quench the generation of dark current electrons via surface states. The PPD is formed by capping the n-well photodiode with a grounded p+ boron pinning implant. The pinning of the photodiode eliminates the normally 100 times greater surface dark current enabling dark currents as low as 10 pA/cm² at room temperature to be achieved. For WFS applications and 24 μm square pixels, it is possible to meet dark current specifications of 0.5 e-/pixel/frame with only modest cooling (-10°C).

The **second** is innovative pixel designs that achieve high conversion (charge to voltage) gains of 66 μV/e-^[32] to 200 μV/e-^[33] to amplify the signal above the noise and obtain effective low read noise of under 2e-. High conversion gains are achieved by reducing the sense node capacitance (including the capacitance of the source follower MOSFET) to below 2 femtoFarad. Low sense node capacitance is achieved by either: 1) isolating the photodiode from its surrounding (mostly by reducing the side-wall capacitance^[32]) in the case of a 3T pixel (left Figure 17), or 2) by using a charge coupled pixel such as a 4T or 5T pixel (middle Figure 17) where charge is transferred similar to a CCD from an image area, the photodiode, through a transfer gate to a low capacitance sense node. These reductions in capacitance are made possible by using 0.18μm or finer CMOS design rules.

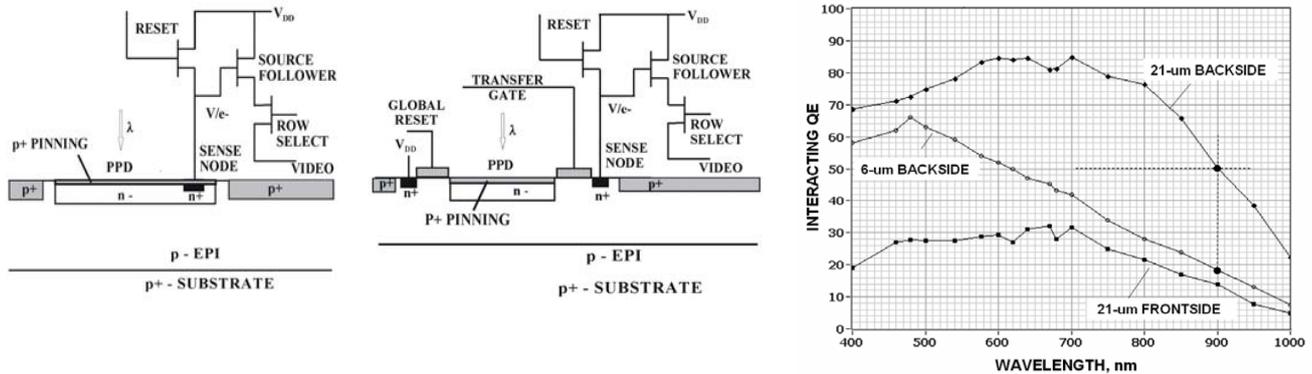


Figure 17: CMOS imager pixels. Left: 3T Pinned Photo Diode (PPD). Middle: 5TPPD charge coupled pixels. Right: First promising results of QE of backside-illuminated CMOS sensor (diagrams courtesy Janesick et. al. [26]).

The **third** innovation is to employ the CCD invention of buried channel MOSFETs to reduce/eliminate random telegraph signal (RTS) noise and background flicker noise associated with the surface states in the source follower (SF) pixel amplifier. Flicker and RTS noise originate through the capture and emission of carriers in traps located at or near the Si-SiO₂ gate interface of the SF amplifier. RTS noise generation usually involves only one or two single traps and single carriers whereas flicker noise arises from the superposition of many RTS sources. As the size of the MOSFET is reduced to decrease its capacitance, RTS noise dominates.

The **fourth** innovation is the improvement in QE and pixel crosstalk of the CMOS imager by back-side illumination^[35] (right Figure 17) and building the sensor from thicker high resistivity silicon (> 10,000 ohm-cm) to efficiently collect

16 Media release Micron Technologies 2006.

charges generated deep within the silicon, without pixel crosstalk and consequential blurring, and to extend the wavelength response into the near red. This is similar to what has been done for Deep Depletion CCDs. There is also talk of adding high voltage ‘substrate biasing’ to generate deep electric fields for much thicker CMOS imagers (referred to as ‘fully depleted imagers’).

The **fifth** innovation is the improvement in charge handling capacity and linearity performance by building into the pixel the possibility to multi-sample the pixel at different conversion gains ($\mu\text{V}/e^-$); e.g. a first sample at high gain to encode the read noise followed by a second one to encode the full well. The different conversion gains can be implemented^[33] by switching in additional capacitance across the sense node of the pixel.

The fundamental difference between CCD and CMOS imagers is that CMOS imagers convert charge into voltage inside every single pixel, whereas CCDs transfer charge one pixel at a time to an output amplifier at the edge of the array that does the conversion of charge (signal) to voltage (i.e., serial readout). To perform this conversion of charge to voltage, CMOS pixels consume only a few μW per pixel (1 μA of current at $\sim 3.3\text{V}$) whereas CCDs require many tens of $\text{mW}/\text{amplifier}$ (1-5 mA of current at $\sim 20\text{V}$). Therefore, it is possible for CMOS to have a highly parallel readout. Typically a few processing channels per column and possibly one per pixel if needed to allow sufficient signal processing and settling time (typically a few micro-seconds per row) to achieve low noise while at the same time performing fast parallel multiplexing and frame readout. This architecture should enable 1680 x 1680 pixel BSI CMOS imagers to achieve $< 2 e^-$ read noise performance at 700 frames/sec readout; generating an overall effective output pixel rate of ~ 2 Gpixels/sec, while consuming modest power of $< 5\text{W}$.

CMOS imagers also have the possibility of using non-destructive read out schemes to take multiple samples of the signal and average them together to “beat down” the read noise. Tried and proven techniques (used standard with IR detectors) such as Fowler sampling (difference of the average of multiple samples taken at start and end of integration) and sampling up the ramp (“linear fitting”) can be employed to achieve sub-electron read noise performance. While this will not be feasible for a fast WFS sampling system ($> 700\text{Hz}$), it could be exploited for slower Tip/Tilt and “Truth” sensors which operate at slower read out speeds of $\sim 100\text{Hz}$.

The other advantage of CMOS is the monolithic integration of circuitry on-chip to provide all biases, sequencer and clocks, and ADCs to reduce off-chip support electronics to a minimum and offer a simple, easy-to-use digital interface.

Polar Coordinate CCD:

The polar coordinate CCD^{[23][24]} is a further example of customizing the detector architecture to the application. The polar coordinate CCD is being developed to be used with both CW and pulsed lasers. As already discussed above, when the number of pixels gets too large, the conventional approach of using a single large format CCD does not work. The pixel rates are too high for the outputs to achieve low noise and the transfer time of the image to store is too long (excessive smearing). To overcome this problem, the polar CCD uses small discrete rectangular arrays of pixels (one small array per sub-aperture), sized and orientated (Figure 18) to optimally sample the elongated spot. This minimizes the number of pixels read out to an acceptable low number and reduces the image to store times to that of the transfer time of the small image array of the sub-aperture.

The polar CCD works with CW laser and is currently proposed to be used in this mode at the TMT for first generation AO systems (NFIRAOS^[25]). However, the real advantage of the polar CCD comes with pulsed lasers when and if they become available. The idea is to track the laser pulse (1-2 μsec pulse) on the CCD by noiselessly transferring the charge on the CCD in the same direction and at the same rate as the laser spot moves across the detector. This is possible as one of the axes of the sub-aperture is designed to be orientated in the direction of the movement of the laser pulse. To deal with varying amounts of elongation as one moves farther away from the laser projection point, the CCD will be broken up into a number of annuli and the image area of each annulus will be clocked independently.

The current development baselines the laser projected from the center of mirror and 60x60 sub-apertures spaced at 500 μm pitch on the detector. The CCD is divided into 10 annuli each with provision for separate clocking. The number of annuli is chosen such that the re-elongation in any sub-aperture from non-optimum clocking is less than 10%. For a CW laser all clocks will be synchronized. For pulse laser tracking, each annulus will be clocked separately to optimally track the pulse. The pixel pitch is 12 μm with the sub-aperture image area varying in size from 6x6 pixels in the central annulus (with least elongation) to 6x15 pixels in the outer most annulus (with most elongation). For the pulsed laser case, it is expected that a maximum of 6x6 pixels per sub-aperture will be read out. Serial registers will snake and tie sub-

apertures together to transfer charge to amplifiers placed at the periphery. In total there will be 128 outputs that use low noise (goal $< 2-3e$ at ~ 3 Mpixel/sec) JFET amplifiers (same type as used on CCID-56) to read the detector at 2000 fps.

Later this year a scaled down demonstrator, 30x30 sub-apertures quadrant with 32 amplifiers, will be fabricated to prove the technology. A test bench will be built to demonstrate the tracking of the pulse; i.e. move a spot across the CCD.

The disadvantage of the polar CCD technology is that a custom CCD will need to be made for each new application, or the application configured or restricted, e.g. use laser center projected and $< 60 \times 60$ sub-apertures, to reuse the existing detector design. The other disadvantage is the scalability. It is unlikely that a 120×120 sub-aperture CW laser version will be practical (too many amplifiers and excessive power dissipation problems). A pulsed laser version with 120×120 sub-apertures may be possible, but could be challenging (512 amplifiers).

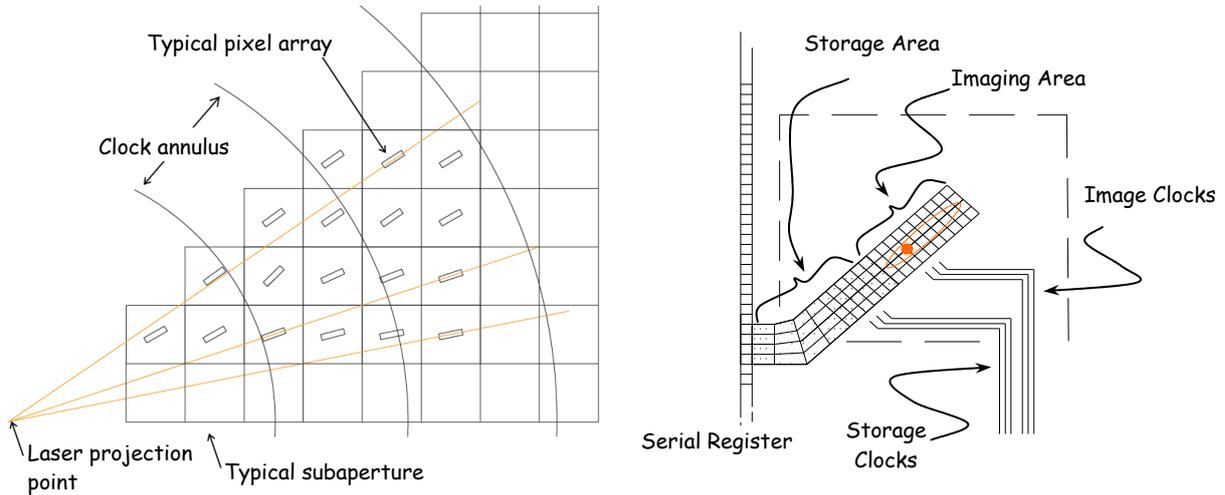


Figure 18: Polar coordinate concept. Left: Each sub-aperture is defined by a polar coordinate system centered on the LGS projection point (hence the name polar CCD). Right: Typical sub-aperture showing how pixels within a sub-aperture are aligned with the orientation of the laser pulse travel (in a radial direction towards the laser projection point). Each sub-aperture is individually aligned (Figure courtesy of Adkins et. al. [22]).

5. IR AO DETECTORS

Due to high read noise (10-20e-) at fast frame rates and poor cosmetic quality, the use of IR detectors for AO applications has been mainly restricted to low order Tip Tilt and “Truth” sensors which require small format size and modest read out speeds of 100 fps. The detectors mostly used for these applications are the PICNIC arrays, the Hawaii-1, and more recently the guide window capability of the HxRG^[38]. Single Correlated Double Sample (CDS) read out noise are ~ 20 e- rms for the PICNIC arrays, and ~ 10 e- rms for the Hx/HxRG arrays. These detectors are scientific sensors that have not been optimized for AO applications.

Table 2 Top level requirements of E-ELT IR AO WFS Detector.

| Parameter | Specification | |
|---|---------------|-------------|
| | Minimum | Goal |
| Array Format (pixels) | 256x256 | |
| Pixel Size (μm) | 18-40 | 40 |
| Wavelength Range (μm) | 0.8-2.5 | |
| Full Frame Rate (fps) | 750 | 1500 |
| Readout Noise (CDS) at 750 fps | < 5 e rms | < 3 e rms |
| Quantum Efficiency at Z, J, H, and K Bands | > 70 % | > 80 % |
| Dark Current (e-/s/pixel at T=80 K) | < 3 | < 1 |
| Storage Capacity (e-) | 10k | 20k |
| Linearity (after flat-fielding) | < 1 % | |
| Photon Response Non-Uniformity (peak-to-peak) | < 10 % | |

For current AO systems and the E-ELT, there is an established need for a much better performing detector (see Table 2 for top level requirements), that is not commercially available and thus requires a custom development. ESO is currently pursuing several options:

Speedster128 and Speedster256¹⁷:

A prototype detector called the CALICO (Figure 19) designed and built by Teledyne was tested at ESO^[39]. This prototype device had 7 different unit cell designs (each 128x16 pixels) and is reported by Teledyne to have a nominal read out noise of 7 e- rms at 800 fps. The most promising design is Lnpix3 which is based on a high gain (responsivity of 1300 mV/e-) Capacitance Trans-Impedance Amplifier (CTIA) pixel architecture.

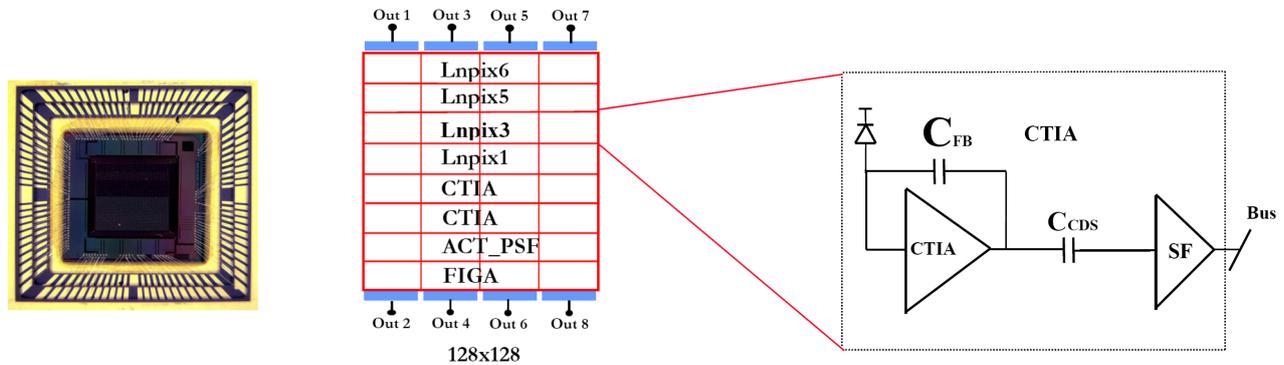


Figure 19: Left: Photograph of AO prototype sensor CALICO. Middle: Chip architecture showing 7 different unit cell designs. Right: Schematic of most promising design, Lnpix3, that is based on a very high gain Capacitance Trans-Impedance Amplifier (CTIA)

Teledyne has taken lessons learnt from CALICO and other IR sensor developments and has developed a new generation of IR WFS arrays called the Speedster128^[40] and Speedster256^[41]. The Speedster128 consists of 128x128 40 μm pixels CMOS readout that can be hybridized to either HgCdTe (1.8 or 2.5 μm cutoff) or Si PIN (0.4-1.0 μm) detector material. The design is targeting read noise of < 5 e- rms in HgCdTe and < 4 e- rms in HyViSI at a read out speed of 900 fps.

The first prototype of the Speedster128 demonstrated chip functionality and good performance at low gain. Unfortunately, the high gain low read noise mode did not work as designed. Speedster256 is the fix of the Speedster128 and has an improved CTIA design as well as an increased format size of 256 x 256 pixels, 12 bit ADC converters on-board, and increased read out speed of 10,000 fps.

e-APDs:

The other path ESO is pursuing is e-APDs. One of the limiting factors of using APDs in the linear region is the excess noise factor, F, which is typically around 2-3 for silicon and 3-5 for III-V materials. The way to overcome this limitation is to operate the APDs at very high gains in the non-linear Geiger mode (with active or passive quenching) and discriminate single photon events (photon counting) to remove the effect of the excess noise.

With APDs made from HgCdTe, excess noise (F) close to 1 in the linear mode for multiplication gains of 100-1000 at low reverse bias of $\sim 10\text{V}$ and bandwidth independent gain has been reported^[42]. These exceptional characteristics in HgCdTe are due to the fact that first, HgCdTe is a direct semiconductor, and second, impact ionization occurs exclusively by electrons (rather than the larger slower less deterministic holes) and thus the name e-APDs. This is in contrast to silicon and III-V materials in which both electrons and holes contribute to the multiplication.

LETI^[42] has recently demonstrated on test photodiode multiplication gains of 5300 at low reverse bias of 12.5V and noise factor of ~ 1.05 -1.3 independent of reverse bias and multiplication gain. There are currently several development on e-APDs^{[44][45]}. ESO is currently pursuing this technology for WFS with SELEX who have developed a 2.5 μm cutoff wavelength prototype detector with a pixel pitch of 24 μm and a format size of 320x256 pixels. The first prototypes are operational and test results^[43] indicate that the device may fulfill the expected noise specifications of an IR AO sensor.

¹⁷ Speedster128 and Speedster256 are trademarks of Teledyne.

6. SUMMARY

This paper has examined the roadmap of optical and infrared detectors by reviewing past detectors, detectors in advanced stage of fabrication/test, and the requirements and status of new detectors whose development are critical for the success of the next generation of extremely large telescopes. Also the paper has reported on the AO WFS detector development and testing programs currently under way at ESO.

During the review of the various AO WFS detector developments, one thing is very clearly demonstrated: the inventiveness of AO WFS detector designers. In many cases this inventiveness has led to custom architectures optimized for the particular AO WFS application. The other surprising thing is the rapid progress in CMOS imagers whose performance now rivals and potentially exceeds those of CCDs. In addition, CMOS imagers have the advantages 1) to integrate additional circuitry on-chip, 2) to address and read out pixels in a very flexible manner, and 3) to accommodate pixels designed with very complicated architectures. Combining advantages with the inventiveness of the AO WFS detector designer, it is easy to see that there exists some exciting times ahead.

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This paper is an update of the one presented at the Marseille SPIE 2008^[28].

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