Implementation of an FPGA-based DCDS video processor for CCD imaging

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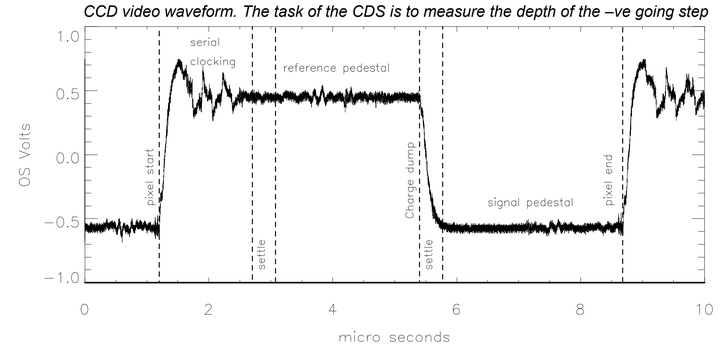
Introduction

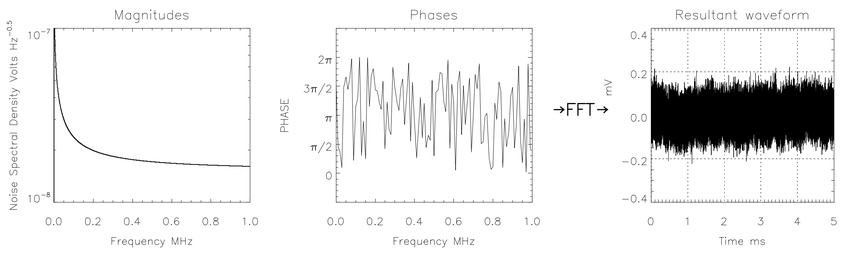
The figure below shows an approximately 1-pixel wide section of a CCD video waveform. The pixel value is the difference between the reference and signal pedestal sections and is measured using a Correlated Double Sampler (CDS) processor. This can be implemented using analogue circuitry or it can be done in the digital domain through the use of a high-speed ADC and an FPGA. In the latter case the processor is known as a Digital CDS. Use of weighted-multiple samples offers the promise of reduced read noise. Modeling was done of the likely performance of various weighted sample schemes and these were then compared with the more traditional "Clamp and Sample" and "Differential Averager" schemes commonly used in analogue processors.

CCD video waveform. The task of the CDS is to measure the depth of the –ve going step

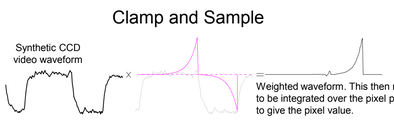


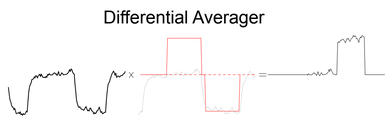
Modeling technique

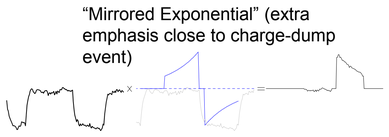
A Fourier technique was used to generate synthetic noise waveforms based on the noise spectrum of the CCD provided by the manufacturer.

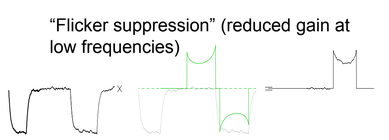


These synthetic waveforms were then repeatedly multiplied by various CDS transfer functions to find the resultant read noise in units of electrons RMS. Four functions or "schemes" were tested. These are shown below.

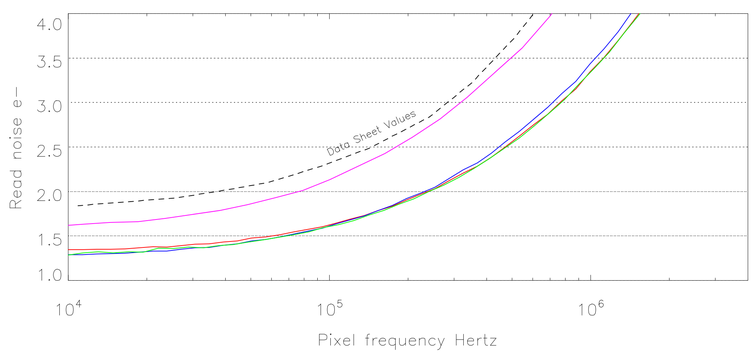






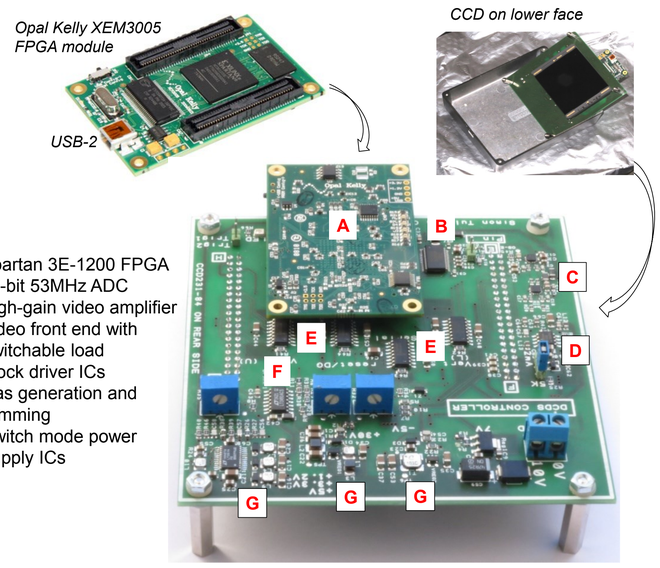


The analysis was repeated over a wide range of pixel rates and compared with the CCD231 data sheet values. The result is shown below. The same color coding is used as in the above graphics. All plots are better than the data sheet values. The differential averager is the best all-round performer.



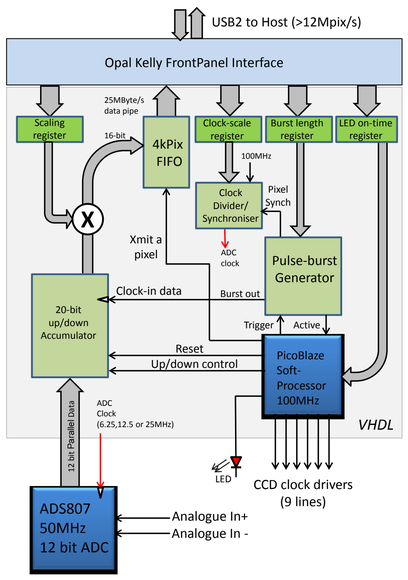
Hardware

A small CCD controller with a DCDS processor was built, first to measure the noise spectrum of the E2V CCD231 and then to check the predictions of the modeling. The CCD was mounted directly onto the controller PCB to minimise extraneous noise sources.

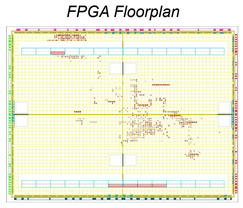


A: Spartan 3E-1200 FPGA
B: 12-bit 53MHz ADC
C: High-gain video amplifier
D: Video front end with switchable load
E: Clock driver ICs
F: Bias generation and trimming
G: Switch mode power supply ICs

A small CCD controller implemented in VHDL. The CCD readout sequencing is done with a PicoBlaze soft processor running at 100MHz. Digital Correlated Double Sampling is done with an up/down accumulator from the Xilinx IP generator library. Processed pixels are transmitted to the host PC via the USB interface. Raw ADC values can also be transmitted to allow the noise spectrum of the CCD to be measured.



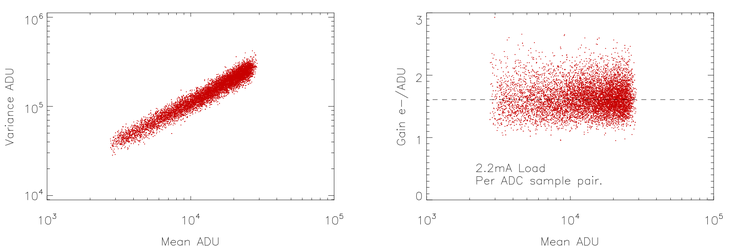
FPGA Floorplan



25% Resource usage

Test image 2304 x 128 pixels. Needed to establish system gain.

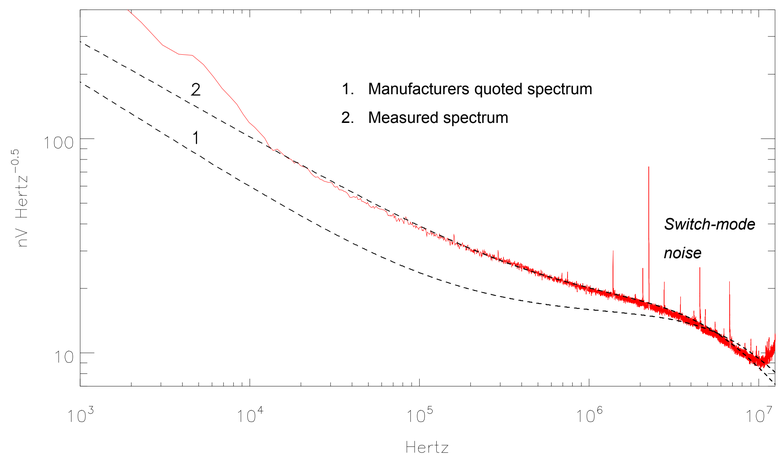
Photon transfer performance, to show that the DCDS processor was well behaved.



Results

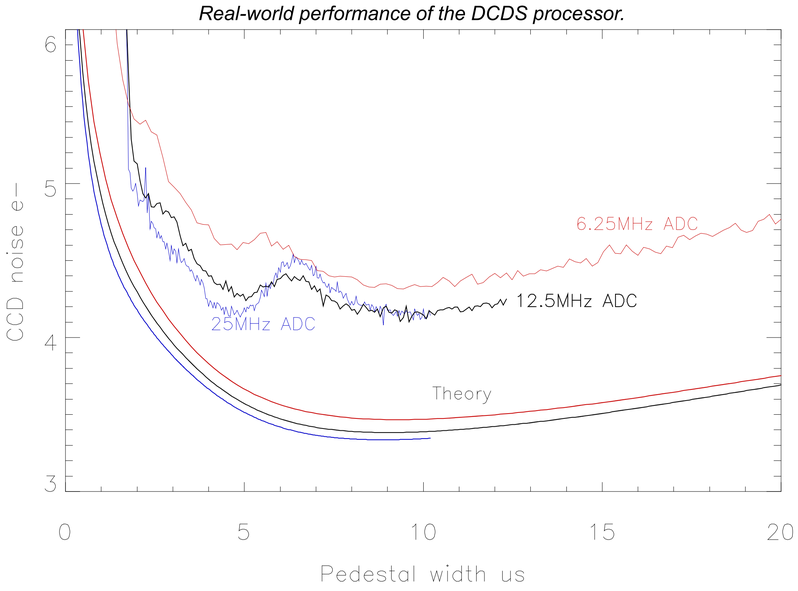
The noise spectrum of the CCD231 was higher than that quoted by E2V. The best fit to the spectrum was given by:

$$N(f) = 15nV.\left(1+\frac{600kHz}{f}\right)^{0.45} VHz^{-0.5}$$



Only the differential averager was implemented in VHDL. Three different ADC frequencies were investigated. The CCD read noise was measured across a wide range of pedestal widths (pixel time ≈ 3 *x* pedestal time). The results are shown below together with the theoretical noise one could expect assuming the measured noise spectrum shown above. The DCDS performance came within 0.8 electrons of theory. Problems with the ADC pipeline were suspected.

Real-world performance of the DCDS processor.



Conclusions

- CCD231 should be capable of lower noise than its data sheet suggests.
- The differential averager CDS scheme is the best all-round performer.
- Weighted sample schemes offer a small 5-10% advantage but only at very low pixel rates. At a systems level this is a negligible improvement.
- Analogue bandwidth shoud be >6 *x* f_{pix}.
- Between 4 and 10 ADC samples are required per pedestal to maximise performance. So, f_{ADC} should be between 12 and 30 *x* f_{pix}.

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Edinburgh, June 2016