ESO Adaptive Optics NGSD/LGSD detector and camera controller for the E-ELT

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ABSTRACT

This paper presents the development of the ESO prototype detector controller for the Adaptive Optics imager on the E-ELT which is based on the e2v Natural Guide Star Detector (NGSD) and Laser Guide Star Detector (LGSD). Both NGSD and LGSD are prototype detectors aiming at proving the CMOS technology in the context of the requirement for a Large Visible AO WFS Detector for the E-ELT. NGSD is a custom design CMOS array detector of 880×840 pixels organized as 44×42 sub-apertures of 20×20 pixel each. NGSD is exactly 1/4 of the LGSD and therefore it is considered a scaled down demonstrator for the LGSD. The detector controller requirements present important challenges in the design of the electronics due to the low-power, low-noise and high parallel data rate of the detectors involved. The general architecture of the controller, the front-end electronics to drive and read-out the detector along with the camera design are described here. This electronics is based on advanced Xilinx FPGAs.

Keywords: NGSD, LGSD, Adaptive Optics, Wave Front Sensing, FPGA, Xilinx Kintex-7, 10-Gigabit Ethernet, 10GEMAC, Ethernet PCS/PMA.

1. INTRODUCTION

In 2006, ESO recognized the need for a Large Visible AO WFS Detector to handle the spot elongation of Laser Guide Stars on the E-ELT. Design studies concluded that the best detector technology to pursue is a large sized high resistivity CMOS Imager. Several years ago, ESO initiated the feasibility study of a 1760×1680 pixels new generation prototype imager called LGSD, Laser Guide Star Detector. Before the development of LGSD, a pioneering quarter size 880×840 pixels Natural Guide Star detector, called NGSD, was built.[1] Both NGSD and LGSD prototypes will have the same pixel architecture and make use of massive parallel Analog-to-Digital structures, as many as 17,600 and 70,400 ADCs for NGSD and LGSD, respectively. In spite of the large size detectors, the frame rate will be above 700 fps and the expected read-out noise below 3 e$^-$. A few samples of the NGSD imager have been produced and for testing purposes ESO has already received and tested[2] both the front-side illuminated and the back-side illuminated versions. The first version of the AO camera and the controller for NGSD is currently under development and aims at: 1. obtaining familiarity with the device (both the front- and back-side illuminated imagers) and, 2. outlining the technology roadmap toward the next generation of ESO controller for AO in the E-ELT era.

2. THE LGSD DETECTOR

The estimated chip size of LGSD is 55×45 mm which makes stitching unavoidable. In order to reduce the line rate (frame period of 1.4 ms, 700 fps nominally), half of the array of LGSD is read upwards and the other half downwards; referred to as the North and South parts, respectively. In addition, to further reduce the line rate, the rows in each half will be read out in groups of 20 in parallel, corresponding to stripes of whole 20×20 sub-apertures (SA) and giving a snapshot shutter within each stripe of sub-apertures.

A detail view of the architecture for both LGSD and NGSD is shown in Figure 1. Both imagers use 20 parallel sets of comparators and registers to read and quantize 20 rows of pixels simultaneously. This feature is needed to achieve the required frame rate and also makes the read of each 20×20 sub-aperture block synchronous within itself. Figure 2 represents the stitching of 4×NGSD that constitutes an LGSD imager.

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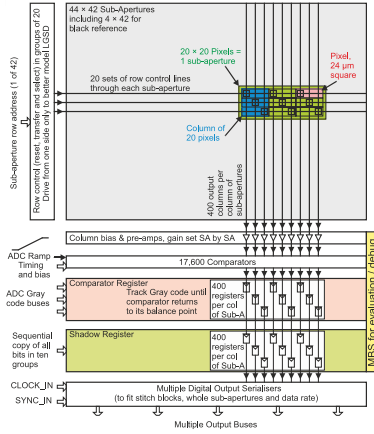
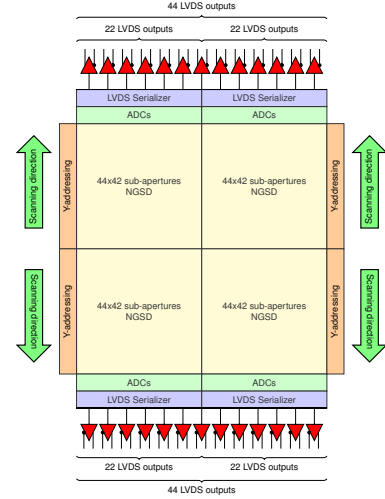Figure 1: Overview of LGSD general plan and data flow.

Figure 2: LGSD geometry depicted as four times NGSD.

3. THE NGSD DETECTOR

NGSD is a quarter cut out of the LGSD and the operation of the two imagers is the same, apart from the numbers of pixels, rows, LVDS outputs, etc. The size of NGSD together with the process test chips and its surroundings is 23.6×30.84 mm. Figure 3 shows the top view of the chip together with the two temperature sensors AD590MF[*] located at the top left and bottom right corners of the chip. The geometry of the 24 μm pixel is shown in Figure 4 where it can be seen the pixel control signals on the left side of the pixel (`Reset`, `Transfer_Gate` and `Select` timing control line gates) and the pixel NMOS transistors at the bottom. Finally, Figure 5 shows a fully packaged chip currently under test at ESO.
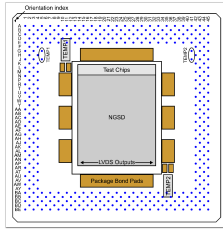

Figure 3: NGSD top view with the two AD590MF[3] temperature sensors.
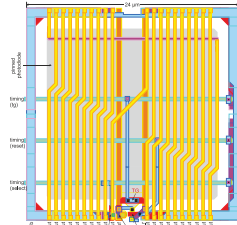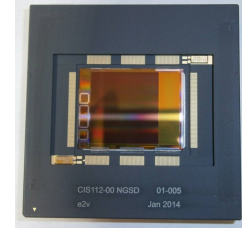

Figure 4: NGSD pixel geometry.

Figure 5: Top view of the BSI NGSD packaged.

4. THE LGSD/NGSD ADC DESIGN AND DETECTOR READOUT SCHEME

Figure 6 shows schematically the 4T pixel structure. At the beginning of an exposure the photodiode is reset to be prepared for the next exposure cycle by activating the `Reset` transistor. At the end of the exposure the charge collected on the pin photodiode is drained by enabling the `Transfer_Gate` transistor and the photodiode signal is transferred to the readout node (represented as n^+ in the figure). The output voltage on the sensing node is measured again after the signal has been transferred by the source follower transistor (biased by `Vsf` voltage in the figure) and presented to the input of the Select transistor. Pixels are individually addressable and presented to the input of the preamp by activating the signals `Select` and `Transfer_Column`. The video voltage signal can be further amplified by the preamp by enabling its gain selection switches and taken to the comparator where

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it is compared with a monotonically growing input ramp until a match is found. Once a match is found the comparator triggers and the value of the counter is latched in a register as the ADC output value. The counter generates values in Gray codes both to minimise the number of edges on the bus into the register bank, as a way to reduce noise coupling, and to guarantee that any match found as the code changes will latch one of the two codes at the transition, and not some spurious bit pattern from a binary change.

Figure 6: Schematic view of the video chain of a single slope ADC.

Each LVDS output sends the data from two columns of sub-apertures. Figure 7 illustrates the architecture of this two-column readout port. All column/rows outputs selected by the Y_ADDRESS (sub-aperture row address uploaded via the SPI serial link during the current sub-aperture read) are copied into a shadow memory register in order to allow the readout of the converted pixels while the next row of sub-apertures is being converted.

In order to simplify the wiring on-chip, the bit order from this block of 40×20 ADCs is such that all bit 0 for first row of ADCs are output first, then all bit 1 for the same row and so on until all bits from the row are transmitted before moving on to the next row of ADCs. This process is further detailed in subsection 7.1.
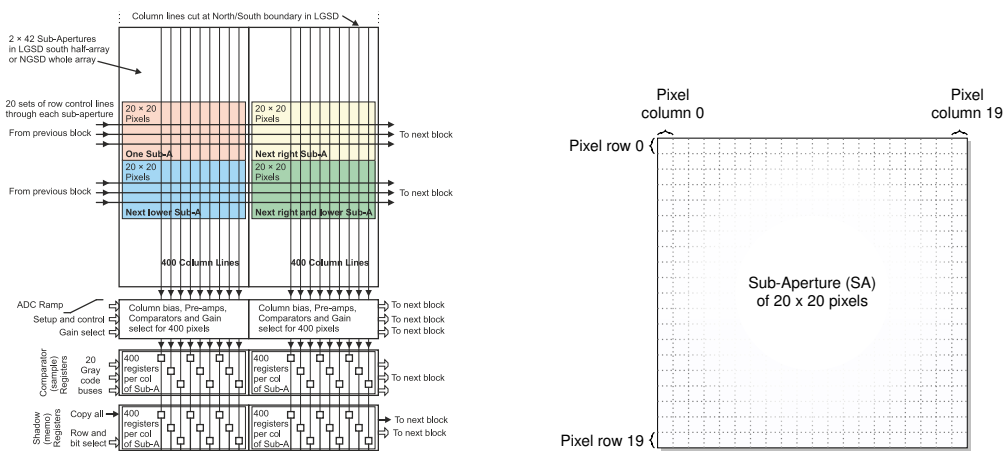

Figure 7: NGSD/LGSD two-column read-out sub-aperture structure and its associated LVDS output.

5. NGSD CAMERA ARCHITECTURE

Since the data conversion and serialization is built-in in the imagers, the camera controller is simplified. For modularity purposes the NGSD prototype camera will internally consist of four different electronic boards: Front-end board, Bias/Housekeeping board, Main board and Back-plane board.

There is no hardwired sequencer in NGSD or LGSD so almost all critical clocks are individually accessible by the FPGA. Thus, the main tasks of the Main board are to provide the pixel timing control of the internal ADCs

(e.g. pixel reset, preset column, transfer column, reset preamp, reset comparators and Gray code generator) and the timing of the LVDS serializers. As an example of the operation, each time a row of sub-apertures is read, its `Y_ADDRESS` must be uploaded over the SPI bus in a data pattern which also includes the gain settings for that row. The SPI runs synchronously to the main data stream readout sequencer process.

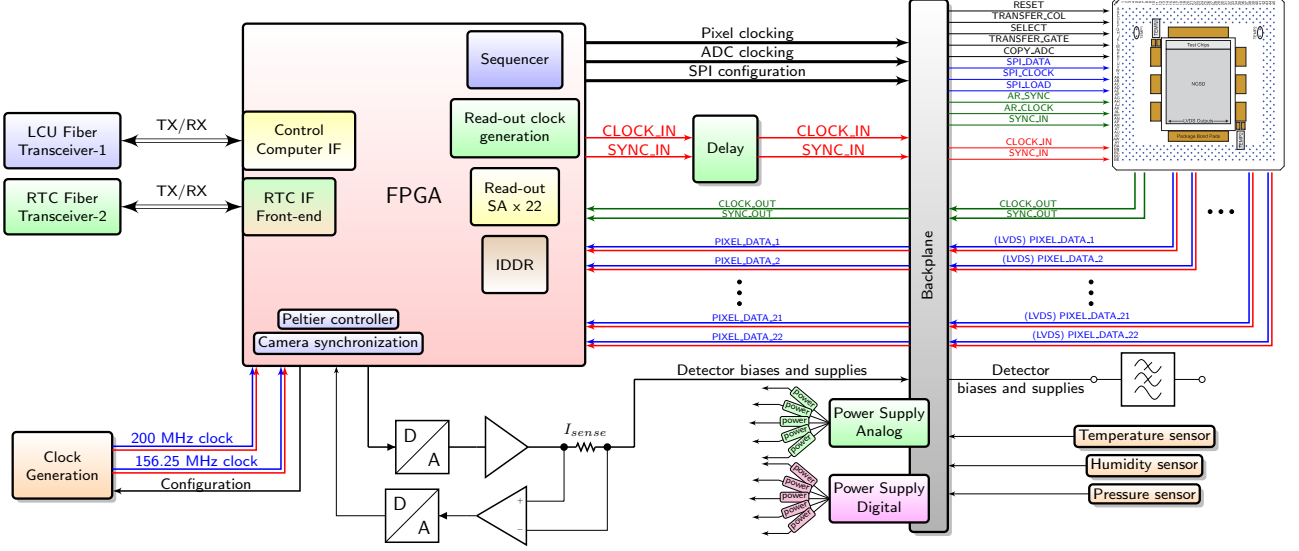Figure 8 shows the main elements of the NGSD controller.

Figure 8: NGSD camera controller architecture.

6. NGSD CONTROLLER

Although the camera controller consists of four different electronic boards, future versions of the camera could easily combine the Front-end board and part of the board Backplane[†] board into one single board. In addition, the Bias/Housekeeping and Main board could be combined into a second single board to reduce the total number of boards to only two. However, it has been decided to implement the first version of the prototype with four boards in order to decouple the different functionalities of the controller and by doing so, ease the testability at the expense of having more interconnects.

To put it briefly, the Front-end board will essentially contain the NGSD chip, the passive filtering of the bias voltages, the wave shaping of the control clock signals and the LVDS output drivers for the outgoing detector pixel stream. The Bias/Housekeeping board will contain the generation of the power supply rails of the active components, the detector bias voltages along with the linear controller of the Peltier element. The Main board is the core of the controller and will host the COTS[‡] FPGA module on which the clock sequencer, the high-speed fiber communication transceiver and many other functions will run. Finally, the Backplane board will contain the voltage regulators for the power supply entry and be the interface between the Main and Bias/Housekeeping boards and the Front-end board. These boards are described on the following sections.

6.1 Front-end board

The detector head is connected to the main board via a 10 cm flex-rigid PCB which has an opening in the middle for the cold finger. The ZIF socket is basically surrounded by passive low-pass filters for the detector power supply and bias inputs. In addition to the low-pass filters, all the incoming clock control signals driving the detector are RC low-pass filtered (i.e. `RESET`, `TRANSFER_COL`, `SELECT`, `TRANSFER_GATE`, `COPY_ADC` and even

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[†]The function of the Backplane board is mainly instrumental as can be seen later and therefore this board could be spared.

[‡]Commercial off-the-shelf.

high-speed control signals like `CLOCK_IN` and `SYNC_IN` described later) in order to limit its bandwidth and avoid excess noise due to unnecessary fast rising and falling edges of the clocks driving the detector.
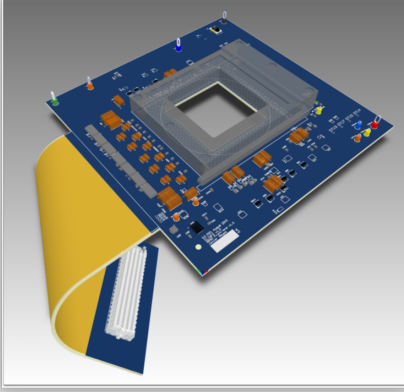

Figure 9: Front-end board.

Just before the flex part of the flex-rigid board, the Front-end board contains LVDS repeaters for each LVDS data stream in order to buffer the detector pixel data output from the FPGA. These repeaters can directly accept LVPECL, HSTL, and SSTL-2 for translation to LVDS so the board covers a wide range of potential CMOS detectors we can have in the future and not only NGSD/LGSD like.

In addition, in order to interface to sub-LVDS standard and reduce the total power consumption, the upper and lower rails of the 22 differential pixel data stream outputs of NGSD can be adjusted via one linear regulator on-board (referred to as `VLOW` for the lower rail) and one programmable upper rail voltage supplied by the Bias/Housekeeping board, referred to as `VHIGH`.

Out of the four boards comprising the controller, the Front-end board is the only one inside a pressurized and dry atmosphere inside the camera head and therefore the board contains humidity, temperature and pressure sensors to sense the environment and provide alarms in case of failure or unsafe operating conditions. The Front-end board is shown in Figure 9, 10 and 11.
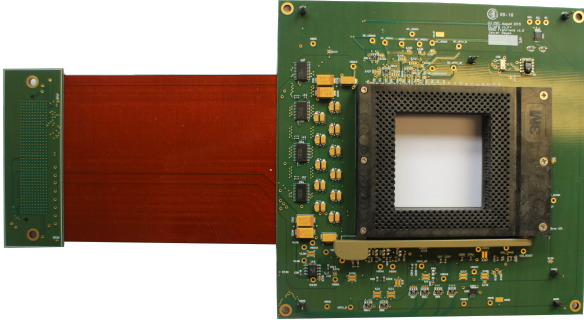

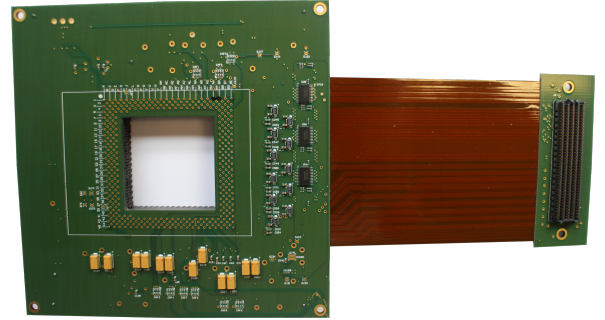Figure 10: Photo of the front of the Front-end board.

Figure 11: Photo of the back of the Front-end board.

6.2 Bias/Housekeeping board

This board provides all supply voltages to the detector and some electronics. It contains three 16-bit resolution DAC modules with eight channel each. The output voltage of each DAC is buffered and low-pass filtered to produce the supply voltage for the detector. The DACs are fully controlled by the FPGA on the Main board and programmable by software.

As part of the detector temperature sensing used to control and stabilize the Peltier element underneath the detector, the board contains the signal conditioning for the two AD590 temperature sensors mounted on the detector package. For supply voltages between 4 V and 30 V, the AD590 temperature sensor acts as a high impedance, constant current source proportional to the absolute temperature with an output conversion of 1 μA/K. On this board the current from each sensor is converted to voltage by a resistor in series, before being amplified, level shifted, and digitized by the ADC on board.
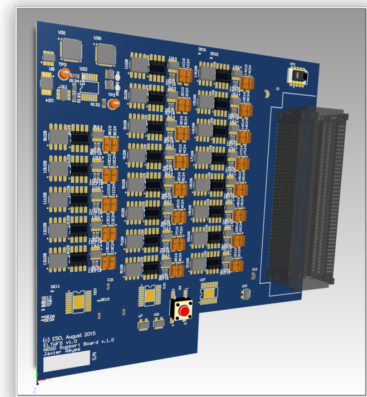

Figure 12: Bias/Housekeeping board.

As part of some telemetry functions provided by the camera, a precision 0.1 Ω resistor is placed in series with each power and bias supply voltage to measure its current. A precision current sense amplifier (MAX4173H) with a fixed differential gain of x100 is used to measure the voltage across the precision resistor.

The Bias/Housekeeping board is located in the camera body (the part of the camera containing the electronics except the Front-end board) in a volume of ambient pressure and humidity which has less demanding dryness requirements. The board provides the environmental sensing functions of humidity and temperature for this part of the camera.
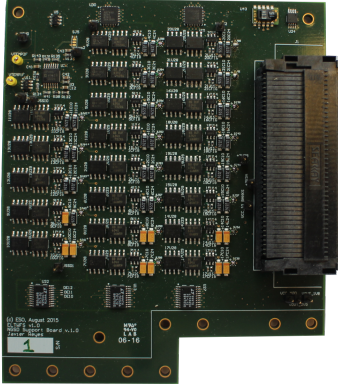
The Bias board is shown in Figure 12, 13 and 14.
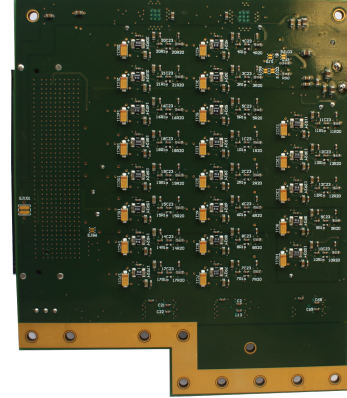

Figure 13: Bias/Housekeeping board top view.

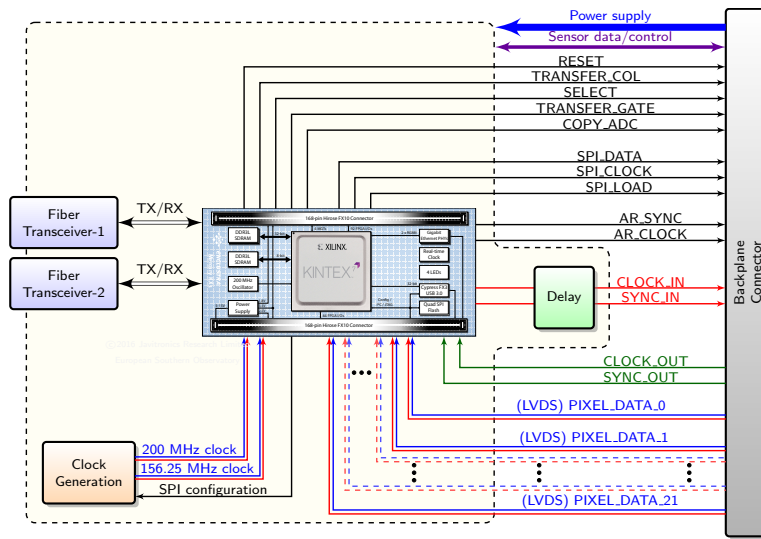Figure 14: Bias/Housekeeping bottom view.

6.3 Main board

Figure 15: Main board block diagram.

Figure 15 depicts the main functions of the Main board. The first version is based on a COTS module from Enclustra[4] containing a Xilinx Kintex[5] XC7K160T-1FBG676C FPGA[§]. The module is piggy-back connected to the Main board via two low-profile and high-density 168-pin connectors from Hirose. The Enclustra Mercury KX1[¶] module is smaller than a credit card and offers multiple standard interfaces; as many as 158 User I/Os (single-ended or differential), up to 2048 MB + 512 MB DDR3 SDRAM and many high-speed DSP slices in conjunction with the latest high-speed standard interfaces like USB 3.0, PCIe 2.0 and Gigabit Ethernet. Figure 16 presents a picture of the module.

The use of a COTS FPGA board instead of integrating the FPGA on the Main board reduces significantly the development effort, redesign risk and improves the prototyping time phase. In addition, since the interface of the FPGA with the outside electronics is via a high-pin count connector with a well-defined and fixed interface, the module on the Main board can be upgraded in the future with a more powerful FPGA by the same company or, in order to save cost and number of interconnects, replaced by an FPGA on-board .

[§]http://www.xilinx.com/products/silicon-devices/fpga/kintex-7.html
[¶]http://www.enclustra.com/en/home/

The basic functionality of the firmware running on the FPGA module is described in section 7.

The power supply for the Main board is provided by the backplane, as shown in Figure 15 and there are not voltage regulators or DC/DC converters on-board with the exception of those on the COTS FPGA module.

The FPGA module accepts an input voltage of +5 V to +15 V and the DC/DC converters on the module deliver +1.8, +2.5 and +3.3 V, these voltages generated on-module are also available on the Main board for general purposes.

The module contains on-board a 200 MHz oscillator which is divided by 2 inside the FPGA and is used to clock the sequencer and some of the internal logic (details further described in section 7), however, for the high-speed fiber transceivers to work at gigabit data rates (from 3.125 to 10 Gbps) it is mandatory to provide externally additional high stability and very low jitter external clocks. The two clock oscillators external to the module run at 200 MHz and 156.25 MHz and are used for the Xilinx Aurora link and the 10 GbE interface, respectively.

As depicted in Figure 15, some of the main functions of this board are:

1. Interfacing with the Local Control Computer (LCU) via the fiber link,
2. Updating the sub-aperture gain and select the column address `Y_ADDRESS` to be read via the signals `SPI_DATA`, `SPI_CLOCK` and `SPI_LOAD`,
3. Providing the clocking of the detector preamp via the signals `RESET`, `TRANSFER_COL`, `SELECT`, `TRANSFER_GATE` and `COPY_ADC`,
4. Controlling of the sub-aperture initialization signals via `AR_SYNC`, `AR_CLOK` and `SYNC_IN`∥,
5. Reading the 22×LVDS pixel data streams,
6. Sending via fiber to the LCU the acquired detector image.

As a result of having the FPGA on a commercial module and easily interchangable, it is however planned to move to faster and more advanced FPGA, e.g. Xilinx Ultrascale or Ultrascale+ technology, if in the future the camera controller requirements are different or the current FPGA is not sufficient to cover the very demanding requirements of a bigger detector like LGSD.

Last but not least, among many other features of the Main board, it is foreseen the provision of circuitry for the synchronization of the camera both to an external trigger or to more than one camera head in order to support future multi-camera scenarios in the E-ELT.

The Main board is shown in Figure 17, 18 and 19.

Figure 16: Enclustra FPGA board. Only 72×54 mm.

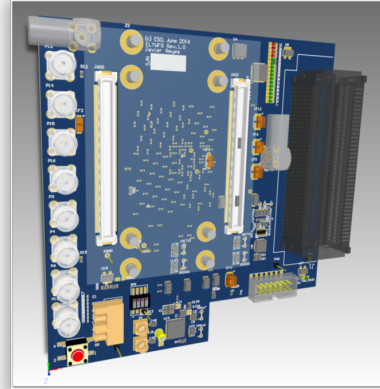Figure 17: Main board.

6.4 Backplane board

∥Both `SYNC_IN` and `CLOCK_IN` going to the detector can be delayed by software in step of 15 ps thanks to a on-board SY89297U programmable delay line.
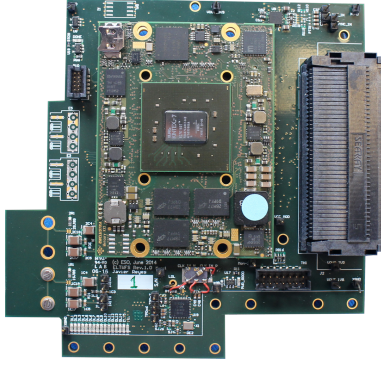
Figure 18: NGSD camera Main board top view.

Figure 19: NGSD camera Main board bottom view.

The backplane is the backbone of the camera and where the Bias, Main and Front-end board are plugged in. The decision on having a backplane on a small AO camera was made in order to facilitate the debugging of all functional components. It is planned to remove this board in future versions of the electronics in order to reduce the number of interconnections and reduce the overall volume of the camera.

Figure 20: Backplane board voltage regulators.

This board serves as the interconnection of the rest of the boards in addition to converting the camera power input to the **raw voltages** required by the rest of the electronic boards. As an example, the raw voltages provided by the backplane to the Bias board are used on the latter as the upper/lower power rails of the op-amps used to provide power and bias signals to the detectors.

There are three input supply voltages of the camera: 1) Positive input voltage that can range from +8 V to +36 V, 2) Negative supply voltage from -8 V to -36 V, 3) Digital supply voltage from +5 V to +18 V. From these input voltages, the backplane generates +5 V, +6 V which are used for the upper rail of the op-amps on the Bias board, +3.3 V logic suppy for, e.g. humidity sensor, but not for the detector, and -5 V for the lower rail of the op-amps used on the Bias board. Figure 20 is an illustration of the voltage regulation on the backplane.
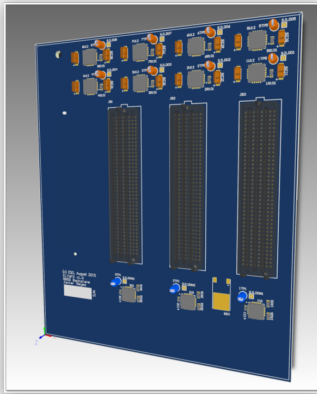

Figure 21: Backplane board.

In the first version of the prototype camera the output raw voltages supplied by the Backplane board are generated by linear voltages regulator in order to avoid any possible noise introduced by more efficient switching mode DC/DC down converter and by doing so, characterize the noise floor of the complete system before doing any natural optimization in terms of compactness, power consumption or components count reduction.

It has been however foreseen that, provided that the performance of the camera is not compromised, the digital supply voltage described above is connected to the positive input supply voltage in order to reduce the three input power supplies mentioned above to only two. This input supply voltage is represented by a dashed line in Figure 20. Furthermore, provided that switching mode DC/DC converters do not introduce additional noise in the system, it is foreseen to replace all the linear voltage regulators by DC/DC converters (even to produce the negative rail) and power up the camera with only one external power supply, e.g. 12 V to 24 V. The Backplane board is shown in Figure 22 and 23.

7. CONTROLLER FIRMWARE OVERVIEW

The firmware running on the FPGA is at the heart of the camera controller. The block diagram of the firmware is depicted in Figure 24.
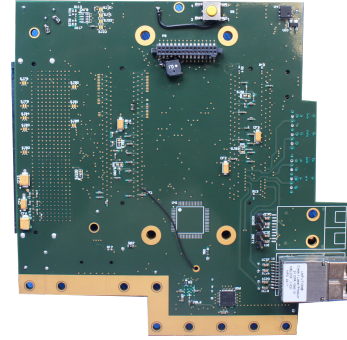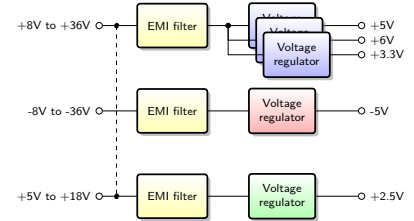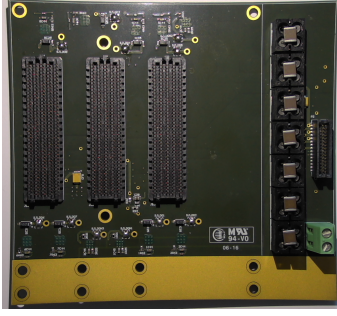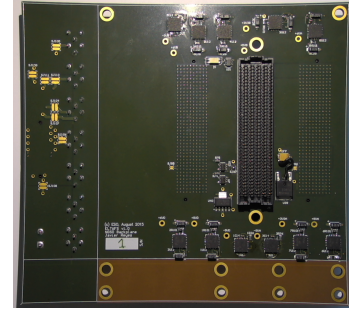
Figure 22: Top view of the Backplane board.

Figure 23: Bottom view of the Backplane board.

There are several clock frequencies inside the firmware but there are basically only two clock domains: 50 MHz and 100 MHz. The 100 MHz clock is derived** from the 200 MHz clock on-board the FPGA module (see subsection 6.3) and is used to clock the sequencer and all the readout acquisition modules/processes which are dealing with the clocking of the detector and the reception of the LVDS pixel data streams. The 50 MHz clock is derived from low-jitter 200 MHz oscillator provided externally to the FPGA module which in the first place is required to clock the multigigabit fiber interface (Xilinx Aurora and Gigabit Ethernet). The 50 MHz is used by the firmware modules/processes dealing with the command and pixel data communication with the remote control and acquisition computer. The 50 MHZ clock domain is mainly to provide compatibility with modules designed for NGC[6] (ESO Next Generation Controller) and can be removed in future revisions of the firmware.

The sequencer that controls the detector clock signals is clocked by the 100 MHz clock mentioned above and therefore has a resolution of 10 ns per tick[††]. The sequencer produces the timing for `RESET`, `TRANSFER_GATE`, `SELECT`, `TRANSFER_COL` and `COPY_ADC` as required for the acquisition of the pixel value as illustrated in Figure 6. In addition to these signals which are directly received by the detector, an internal sequencer signal called `SPI_SETUP` updates the detector SPI register with the `Y_ADDRESS` and the `GAIN` for the row of sub-apertures ready to be converted. See previous Figure 7.

The detector signal `COPY_ADC`, which produces the transferring of the all the 400×ADCs per sup-aperture column into the internal detector shadow register inside the detector, also triggers the firmware block clock called Read-out sub-aperture control in Figure 24 which is responsible for reading all 22×high-speed LVDS ports.

The firmware process Read-out sub-aperture control controls the low-level process called Read-out sub-aperture. The working principle of the Read-out sub-aperture firmware process is explained in subsection 7.1. The individual pixel data streams are connected to internal memory RAM, sorted by dedicated logic, converted from Gray code to binary and combined before being sent to the Real-Time-Computer (RTC) for processing.

7.1 Firmware read-out scheme

The pixel data from each block of two sub-apertures of 20×20 pixels each, i.e. 800×ADCs, is sent by the serializer through a single LVDS port in the order represented in Figure 25. In case of 9-bit per pixel ADC configuration a total of 800 pixels × 9-bit = 7200 bits is sent to the FPGA per LVDS port. The transmission is such that the serializer will output first bit-0 of the first row of 40 pixels, followed by bit-1 of the same row until bit-9 from the same row is been transmitted before moving on to the next row of ADCs.

The pixel receiver inside the FPGA receives the pixel bits transmitted by the serializer synchronously to the `CLOCK_OUT` signal and the input signal `SYNC_OUT` marks the beginning of the first bit of the first pixel of one row of pixels. From the FPGA point of view the bit stream is passed through a DDR (Double Data Rate) FPGA input primitive to obtain two pixel bits per `CLOCK_OUT` period. These bits are dispatched to an Even/Odd bank

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**The MMCM block in Figure 24 stands for mixed-mode clock manager in Xilinx terminology. It serves basically as a clock synthesizer inside the FPGA.

††This resolution can be easily increased to 5 ns resolution per tick by using DDR primitives internal to the FPGA as on the ESO AOWFS camera[7] but it has been found unnecessary for the moment.
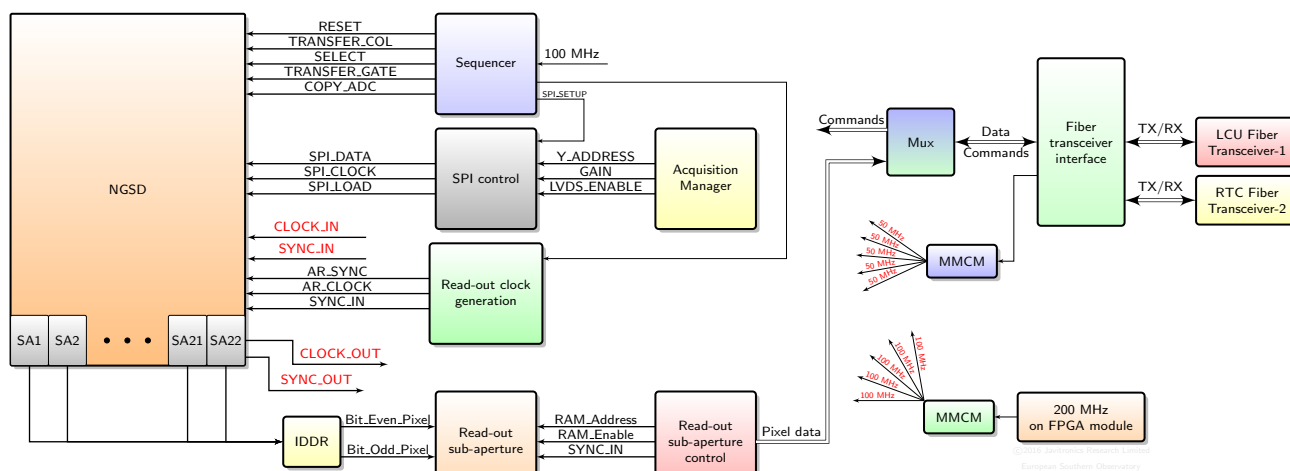
Figure 24: Firmware architecture.
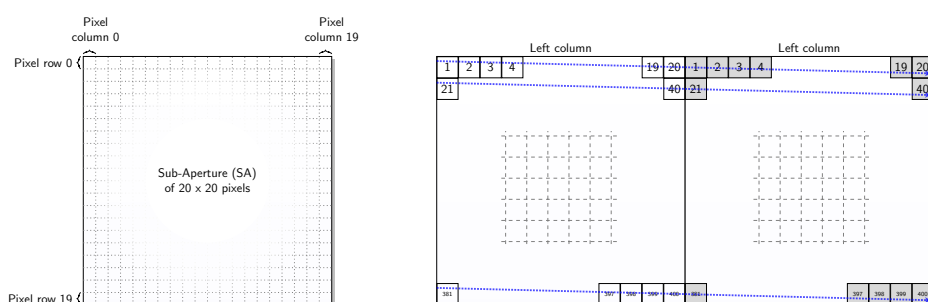
Figure 25: Numbering of pixels within each sub-aperture and NGSD readout order for two sub-apertures.

of RAMs for storage and later read-out, pixel composition, conversion from Gray to binary and transmission to the RTC. This process is represented in Figure 26.
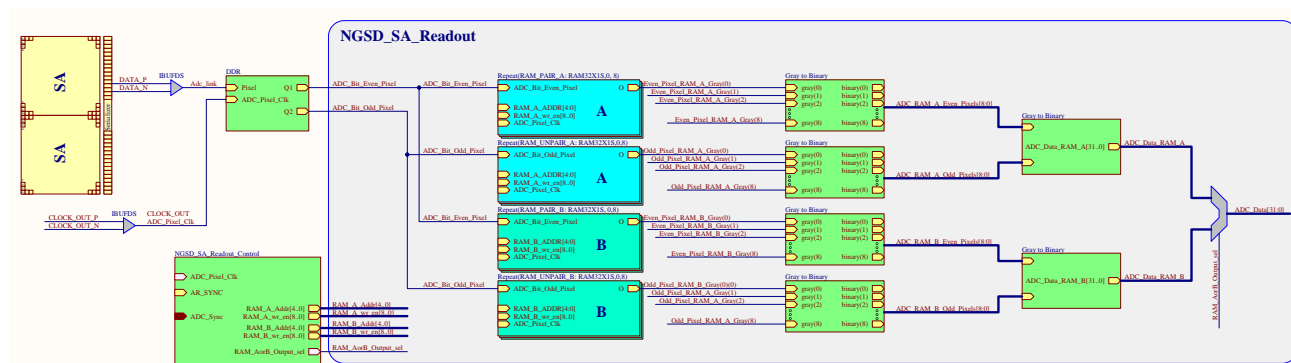
Figure 26: Firmware block diagram to read-out one SA.

The overall timing to set-up the SPI register, read the image and transfer the data is shown in Figure 27.

As mentioned earlier the ADC is based on a Gray code counter incrementing until a match is found by the comparator between the video signal to be measured and the incrementing ramp. It may appear very elaborate and time consuming to convert the Gray code to binary but this operation is in nature very simple and does not consume many resources from a firmware point of view. The 9-bit Gray code conversion to binary is performed

in the FPGA by cascading XOR gates as shown in Figure 28. This operation is combinational and done within one clock cycle of the main pixel clock.
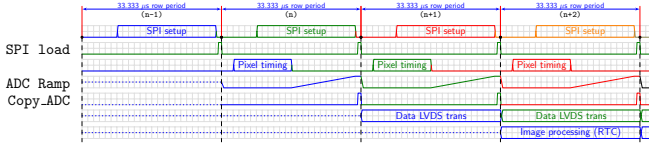
Figure 27: Timing diagram for image read and data output.
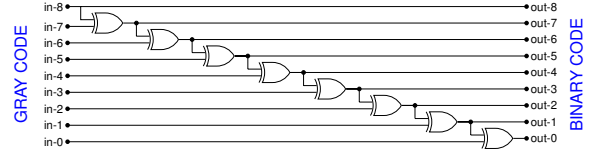
Figure 28: Gray code to binary translation done in the firmware.

8. SOME OTHER ASPECTS OF THE E-ELT AO CAMERA

8.1 Connection to the RTC

The design of the RTC for ESO's E-ELT instruments is still under definition and feasibility study, but the interface to the controller will be 10GbE using UDP-based protocol or RTSP (Real-Time Streaming Protocol) on top of it in order to allow data broadcasting.[8] The use of 10GbE links for the interface will allow high-performance point-to-point and multicast through Layer 2 Commercial off-the-shelf (COTS) network switches which have already been proven to perform deterministically without packet losses. Layer 2 switching is hardware based, mostly based on ASICs, which means that the latency is very low and switching is highly efficient because there is no modification to the data packet, only to the frame encapsulation of the packet.

8.2 Gigabit Ethernet

In the context of the 10GbE validation and as part of the forthcoming controller development definition, preliminary tests were carried out successfully by Jorge Romero[9] to run point-to-point data transmission using UDP/IP using the high-speed GTX serial transceivers on a Virtex-6 FPGA. The UPD/IP firmware has been developed from scratch and tested in loopback mode over fiber link at 6.25Gbps. The end-to-end packet latency is of about 47ns. In addition, 10-Gigabit Ethernet packet transmission via fiber has been demonstrated on a Virtex-7 through PHY layer (PCS/PMA) and a latency measured of about 310 ns has been measured and reported.

8.3 Operation homogeneity

It is not a minor goal requirement within ESO that the user of a new controller experiences no significant difference with previously used/deployed detector controllers. It is therefore important to point out that, in spite of the vast variety of detectors operated by ESO, both NGSD and LGSD AO cameras will be operated at the user level similarly to current suit of cameras like AONGC and ScNGC (usually referred to Scientific-NGC). Figure 29 and 30 show the control interface GUI and the software widely used to program the FPGA sequencer .

9. CAMERA MECHANICS

The camera mechanical design has been conceived in two well differentiated parts, the part containing the Front-end board on which the detector is mounted, referred to as camera head, and the part containing the rest of the electronic boards and its interconnection to the outside world, referred to as camera body. See Figure 31. This division has mainly two important advantages. Firstly, it allows the decoupling of the camera body from the camera head which is sealed and pressurized. This decoupling permits the maintenance and replacement of only one half of the camera without affecting the other half. Secondly, it eases the high-speed data connection of the electronics inside the camera body (mainly the fiber connections from the Main board to the RTC and control computer) without special and usually very expensive high-speed fiber feedthroughs.

Figure 29: ESO camera control GUI software.

Figure 30: BlueWave to program the timing pattern for AONGC, ScNGC and future E-ELT NGSD/LGSD controller.

The division of the camera between head and body is done by the cooling block which can be thought as the mechanical backbone of the camera; with the camera head and body attached to each side of it. The cooling block has the connectors for the water cooling to which the cold finger, going to the bottom side of the detector, is attached via thermal bellows. In addition to providing cooling power to the back of the NGSD detector, the cooling blocks provides fins where the electronics boards (Bias/Housekeeping, Main and Backplane board) are bolted and thermally connected. All these details are illustrated in Figure 32.

Figure 31: 3D view of the ESO camera for NGSD.

Figure 32: Cooling block assembly illustrating how the camera head and body are divided.

Similar to the current ESO AOWFS camera[10] based on the CCD220, it is expected that the NGSD/LGSD camera head will be sealed air tight and flooded with nitrogen. The pressure inside will be slightly above the atmospheric pressure in order to avoid the ingress of moisture inside the camera head resulting in water condensation. As for the ESO AO camera, this camera will have pressure, humidity and temperature sensors in addition to dedicated over-temperature and over-voltage protection circuitry.

The arrangement of the boards inside the camera is illustrated in Figure 33. All the interfaces of the camera are placed on the back panel, see Figure 34.

The dimensions of the first prototype of the camera is $128 \times 143 \times 145$ mm^3 (W$\times$H$\times$D), and the weight is still TBD. The current dimensions can be further reduced if the slot for the Reserved board (Figure 31) is removed

and the Front-end board dimensions are reduced by folding the PCB as shown in Figure 35, this would produce and estimated camera volume of about $128\times143\times118$ mm^3.
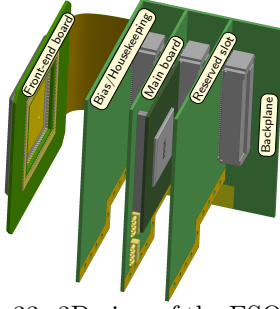

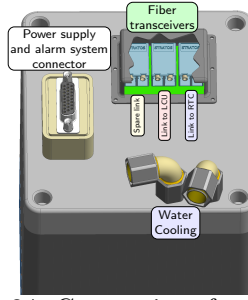Figure 33: 3D view of the ESO camera for NGSD.

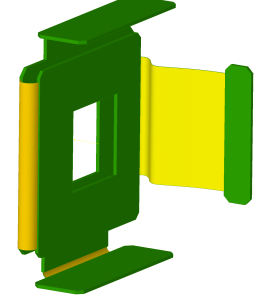Figure 34: Camera interfaces on the back panel.

Figure 35: Front-end board with folded flex-rigid PCBs.

9.1 PELTIER CONTROLLER

Both NGSD and LGSD must be cooled to the temperature that satisfies the required dark current. This temperature is in the order of -20 degC in operation. The Peltier controller will be part of the demonstration camera and it is planned to have an integrated Peltier controller in order to reduce the number of components and improve the overall dimensions of the camera. It is estimated that 8 V and about 3 A will be sufficient to cool down the NGSD detector to -20 degC with water cooling between 25 and 30 degC. The design of the Peltier controller will be based on a 32-bit embedded soft processor inside the FPGA (Xilinx Microblaze[11]).

10. SUMMARY

NGSD Detector technology	e2v CMOS	Total Throughput	5Gb/s approx.
LGSD Detector technology	e2v CMOS	Total Throughput	20Gb/s approx.
Format NGSD	880×840 pixels (44×42 SA)	SPI Configuration	Up to 10Mb/s
Format LGSD	1760×1680 pixels (88×84 SA)	FPGA	Xilinx Kintex XC7K160T
Pixel size	24×24 m2	Sequencer	2.5ns ticks, 78ps resolution
RON	< 3e- (<1e- for Ultra Low Vt)	Link to PC	1310nm fiber, 3.125Gb/s
Frame rate	700 fps nominal, Row time: 1.4ms	Link to RTC NGSD	UDP 10GbE
		Link to RTC LGSD	UDP 4x10GbE (RTSP goal)
On chip ADC	9-bit (10-bit optional) Gray code	Temperature	-20 degC
Sub-aperture gain	x1, 2, 4 and 8	Cooling	Peltier
NGSD pixel stream output	22×LVDS	Gas filling	Nitrogen flushed
LGSD pixel stream output	88×LVDS		
LVDS Bit Rate	216 Mb/s	Peltier	Controller integrated on FPGA

Table 1: Summary of main technical specifications.

11. CONCLUSION

This paper introduces the two new large format CMOS imagers on which the ESO's E-ELT Adaptive Optics may be based along with some implementation details of the prototype controller under development. The controller presented here will be crucial for ESO to gain experience with the prototype NGSD detector and to deepen the knowledge on any new CMOS imager the future E-ELT AO camera may be based upon. Moreover, this controller also aims to underpin with much of today technology the requirements and possibilities of a future full size (LGSD like) AO detector controller for the E-ELT.

Although very promising results have been obtained during the testing of NGSD,[1] ESO has initiated a procurement process to select the industrial partner for the production of the final E-ELT CMOS imager in order to solve the remaining issues encountered on the current NGSD prototype imager. In the context of foreseeing the adoption of an imager different than NGSD for the Adaptive Optics of ESO's E-ELT, both the camera and the detector controller have been carefully conceived with special focus on modularity and adaptability to any new large CMOS Imager this second iteration may bring.

12. FUTURE WORK. THE LGSD CONTROLLER DEMONSTRATOR

The LGSD detector is four times the size of NGSD and the scalability of the controller from NGSD to LGSD presents additional challenges in itself, such as the electronics power consumption in a small volume and huge data throughput transmission to fulfill the required frame rate. The experience acquired in the development of the NGSD controller and the testing of the detector will serve to outline the design of the future controller demonstrator for LGSD and its associated tools.

ACKNOWLEDGMENTS

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