Performance and evaluation of the infrared AO sensor CALICO

,

Leander H. Mehrgan*, Siegfried Eschbaumer, Gert Finger, Manfred Meyer, and Joerg Stegmeier
European Southern Observatory, Karl-Schwarzschild Str. 2, D-85748 Garching, Germany

ABSTRACT

The CALICO sensor is a pathfinder for the development of the future infrared high speed low noise detectors for AO. Low readout noise at high readout speed is accomplished by high gain and signal processing circuitry under each pixel. The high gain makes the detector very susceptible to instability if the system noise is too high. Lnpix3, the most promising structure, has a pixel gain of 400. In this paper we will report on test results and different measures we had to take getting the detector to work.

Keywords: wavefront sensor, low noise, read noise, high speed detector, Adaptive Optics

1. INTRODUCTION

To improve the performance of the VLTI fringe tracker FINITO and to investigate the best unit cell circuit for future infrared wavefront sensors, ESO has teamed up with CALTECH and placed a contract with Teledyne (former Rockwell) to develop a new 2.5 micron cutoff HgCdTe prototype sensor: the CALICO chip. It has 7 different unit cell designs. The goal of this development is to select the best design to manufacture a uniform small format 256x256 AO wave front sensor. By placing the signal processing circuitry under each pixel it is possible to filter the noise prior to multiplexing. The CALICO sensor has 8 parallel video outputs and can be operated at a frame rate of 2.71 KHz.

2. STRUCTURE OF THE CALCIO DETECTOR

This detector is designed as a prototype containing 7 different unit cell designs. All designs have at least one or more gain stages in the detector pixel. Traditional inverting amplifier gain stages as well as gate modulation based ultra high gain stages are implemented. This multiple design approach helps with trade-offs in the large design space comprised of requirements such as linearity, power dissipation, full well capacity and detector capacitance, and to pick the optimal solution with the lowest noise. The ROIC is implemented in a 0.25µm mixed signal process with a 40µm pixel pitch. Test features such as charge injection capacitor arrays are incorporated to calibrate circuit performance. All the bias voltages are internally generated from a single external master bias voltage. Two bias modes are incorporated to auto-bias the circuitry at 300K or 80K. The ROIC has on-chip power decoupling to improve power supply noise pickup rejection. Internal bias and power decoupling are extremely important in achieving ultra low noise by decoupling the sensor from external noise sources on the board. The left picture in Figure 1 shows the CALICO device, which has been used for the evaluation of the CALICO detector. On the right side of Figure 1 we see the conceptual die floor plan of the CALICO [1].

Figure 1 on the left the CALICO IR device, on the right the conceptual die floor-plan showing 7 different pixel designs.

* lmehrgan@eso.org ; phone +49-89-32006204; +49-89-3200272; fax +49-89-3202362;www.eso.org

The CALICO detector has been designed with the following features:

- Array size: 128x128 (40 um pixel)
- Seven unit cell designs
- 8 output channels
- 7 MHz readout rate per output; double data rate (DDR) with 3.5 MHz clock
- Frame rate of 2.7 KHz
- Three output buffer types, also one without buffering
- On-chip auto reference generator
- 2-wire serial interface to select design cells

Different pixel design specs are shown in Table 1.

Design	Approaches	Noise @ 80 K (VIS/IR)	Con. Gain	Issues
ACT	Source follower with CDS and gate modulation	3.5/16.2 e @ 5fF/ 30fF	Current integration	Bias for gate modulation stage
FIGA	Front end voltage gain stage with gate Modulation	3.9/10.6 e	Current integration	Slow for IR diode, low noise bias
CTIA	CTIA front with CDS and gate modulation	3.1 / 6.7 e	Current integration	Low noise bias
Lnpix6	Detector integration with 2 gain stages and CDS	4.9/12.7 e	0.8/0.4mV/e	Need two large Caps
Lnpix5	CTIA stage at front with CDS and gain stage at back	3.7 / 7.3 e	1.3mV/e	Amplifier 1/f noise may limit the noise Level
Lnpix3	CTIA stage at front with CDS and 2th gain stage	3.7 / 7.7e-	1.3mV/e	
Lnpix1	Detector integration with SF/CDS and CTIA gain stage	6.7/29e	1/0.2 mV/e	

Table 1 Summary of all 7 cell designs of the CALICO

3. LNPIX3 DESIGN

In this paper we concentrated on the evaluation of the LNPIX3 design because of its low noise. The design is based on two amplifying gain stages followed by a source follower readout amplifier in the pixel. Figure 2 shows the simplified block schema of Lnpix3. The first stage is a capacitive trans-impedance (CTIA) amplifier and the second stage is an inverting capacitive feedback amplifier. The second stage amplifier combines the functions of band limiting the CTIA, signal amplification and CDS. This provides a compact low power design capable of achieving ultra low noise at high frame rates. This all makes Lnpix3 the most promising structure because of its linearity, its high gain and its low noise. Here again the summary of features of Lnpix3:

- Low noise: 7.7e- (30fF) (80K),
- High total gain: (1300uV/e-)
- Suppresses KTC noise and amp 1/f noise
- 2 stage design – 1st stage is CTIA; 2nd stage is inverting capacitive feedback amplifier; in-pixel CDS; source follower amp for readout
- Compact, low power and ultra-low noise with an effective gain of 1.3 mV/e.

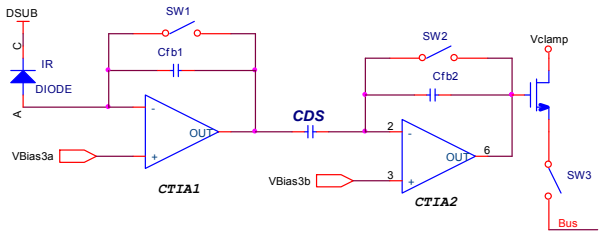

Figure 2 simplified block scheme for Lnpix3 design

Each CTIA stage has a gain of about 20 yielding a total gain is 400. The switches are fully controlled by the internal circuit and cannot be changed manually from the outside.

3.1 CTIA Design

An advantage of the CTIA-based LNPIX3 unit cell design is that the bias across the photodiode is kept constant. The photocurrent is directly integrated on the feedback capacitor. The output of CTIA goes through a large swing during an integration period. The reduction in the input impedance due to the large gain in the amplifier also boosts the injection efficiency, thus allowing extremely small currents to be integrated [1].

4. TEST SYSTEM

In order to install this detector in an already existing instrument the size of the detector board had to comply with the existing set-up [3]. The array was read-out with the ESO data acquisition system for IR detectors IRACE [4]. For the CALICO an 8-channel system with an AD-converter of 2 MSPS was used. To be able to operate the detector at high video speed and at cryogenic temperatures the opa2350 from Burr-Brown (Texas Instrument) was chosen. This amplifier provides:

- low power consumption
- high slave rate
- working at cryogenic temperature
- low noise
- Rail-to-Rail output.

Two different cryogenic set- ups have been used, one portable set-up without imaging optics and one camera with a cold pupil and a filter wheel at cryogenic temperature (IRATEC). That camera uses an f#/11 Offner relay. The filter wheel offers the selection of several astronomical band-pass filters. The portable bath cryostat has no optics but a fixed H-band filter and a focal ratio of f#/3.2 at detector. The transmission curve of the H-band filter is shown in Figure 3.

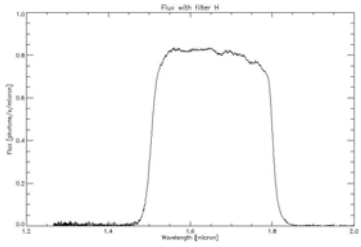

Figure 3 Transmission curve of the H-band filter

The two camera systems are shown in Figure 4. In the back we see the compact IRATEC camera and in front of it in gold color the bath cryostat.

Figure 4 Test camera systems

4.1 Detector controller system IRACE

The ESO data acquisition system for infrared instruments, IRACE, has been used for the developing and testing of the CALICO detector. A picture of the IRACE 8-channel data acquisition system is shown in Figure 5. The front-end electronics of IRACE contains two ADC boards each equipped with 4 ADCs with a speed of 2 MSPS. In addition one module for data transport (Giga board) and two other boards for generating the control signals like clocks and biases were installed. The data transport to the Linux PC is done via fiber optic connected to a custom made PCI card. The data processing machine is a 19 inch rack mountable PC with two Intel-Xeon 3.0 GHz CPUs, 3 GB memory within a system bus of 400 MHz (FSB).

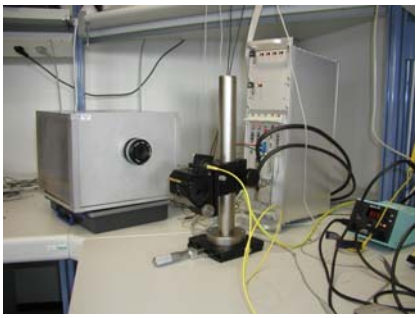

Figure 5 Test bench for testing of the bare mux within a point light source, including IRACE front-end electronic

5. INITIAL PROBLEMS

At the beginning we faced several problems to get the CALICO bare mux working. Due to incomplete documentation several pin assignments on the detector board were wrong. This caused several short circuits and consequently the power voltage broke down. After correction of those pin miss-assignments we could get the first light. Figure 6 shows the output of all seven designs obtained with the CALICO bar mux. The fact that the bare mux was not damaged in spite of that serious mistake is an indication for a well down protection circuit and a robust design. The next important problem was the speed of the video output. To run the CALICO detector at a speed of 7 MHz we should have a video output signal with at least a raise and fall time of about 30 ns, but it was much slower, about 280 ns. For IR detectors we use a symmetric CMOS preamplifier directly on the detector board operating at cryogenic temperature, which among others facilitates the use of long cables and rejects pickup noise. Since the on-board preamplifier is only a distance of a few millimeters from the detector we connected to the unbuffered output of the CALICO detector. The CALICO detector provides two different output amplifiers. Using the buffered output significantly improved the speed of the video output. Fine tuning of the control signal for the output buffer and finally running the detector at cryogenic temperature resulted in the expected high speed video output. The main problem came up when we ran the IR detector at the cryogenic temperature. Using the same setup as the bare mux led to unstable output response from the IR detector at cryogenic temperature. This was solved by implementing various improvements in the test system design.

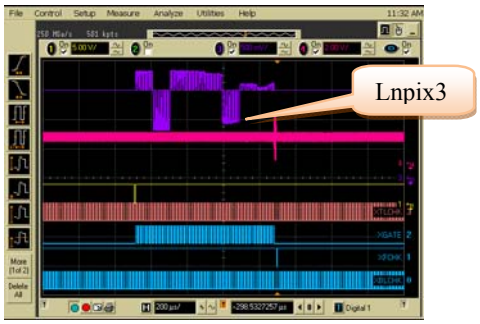

Figure 6 Video output of all seven deigns with the CALICO bare mux

5.1 Stability of the video output of the Lnpix3 structure

As shown in Figure 2 the Lnpix3 design is based on two amplifying gain stages with a total pixel gain of about 400. The high pixel gain makes it very sensitive to the system noise. The voltage reference of the first stage (called vbias3a), which is the counterpart voltage to the detector substrate voltage DSUB, can either be forced by the control electronics or by default be generated by CALICO. Just as an example to illustrate the sensitivity of the circuit to the system noise, if for instance the reference voltage vbias3a would have a noise superimposition with an amplitude of 1mV then this would be amplified and after the second stage would come out with a noise amplitude of 400 mV, which is quite a lot. To keep the system stable at all voltages, even the internally generated voltages have to be kept clean by external filtering. The following actions have been taken to get the detector stable:

- Disconnecting the reference voltage of the first stage (vbias3a) from the control electronics IRACE.
  The reference voltage should be generated internally and not being forced from outside. By putting several capacities in parallel between vbias3a and DSUB voltage this can be well filtered.
- Using of short cables both inside the Dewar and outside for the connection to the control electronics.
  This reduces the influence of the pick-up noise.
- Disable all unused cell designs.
  Actually each cell design can be selected by programming the internal register. Deselecting unused cell designs was not sufficient. They should be powered down by setting some control voltages.
- Robust and massive ground connection, as well as shielding and an additional ground layer for the detector board.
  Additional ground layer in the detector board and also in the flex cable helped to reduce the system noise.
- Fine tuning of some voltages to bring the detector in a stable state.
  Lnpix3 worked well within a narrow range of voltage setting.

In Figure 7 the pixels of the Lnpix3 structure are show with a point source imaged onto the detector. The signals on the oscilloscope are the differential output of the detector, generated by the on-board pre amplifier (green and yellow traces).The oscilloscope's picture shows the video output of one channel while the CALICO detector has eight parallel output channels.

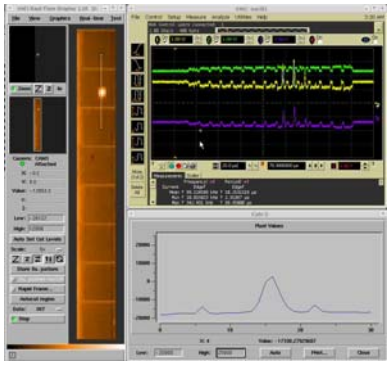
Figure 7 Light point source displayed on RTD and oscilloscope

6. PERFORMANCE CHARACTERIZATION

6.1 Linearity

The Lnpix3 design has two gain stages, so the linearity of the output signal is also an issue of the amplification of the input signal. The variation of the voltage reference of the second stage, vibias3b, shows a dependency of the signal linearity on vbias3b. The higher the bias voltage vbias3b the more linear is the output signal. Unfortunately more linearity, by increasing of vbias3b, is on expense of more noise. This behavior is shown in Figure 8. We could obtain the best linearity behavior and a reasonable noise, which is a compromise, with a voltage value of 0.85 volts. In addition to that a CTIA circuit in general tends to non-linearity at very short integration times. This is due to the fact that the CTIA amplifier takes some time to settle after reset. This behavior is also modeled and shown in a figure in the CALICO paper published at SPIE. Thus the right way to do the linearity measurement is at a fixed integration time varying the flux. Preferably the integration time should be large so we don't get any second order effects due to CTIA's incomplete settling. A minimum integration time of 200us with a pixel clock of 2 MHz, which is the maximal speed setting of our data acquisition system, avoids the non-linearity.

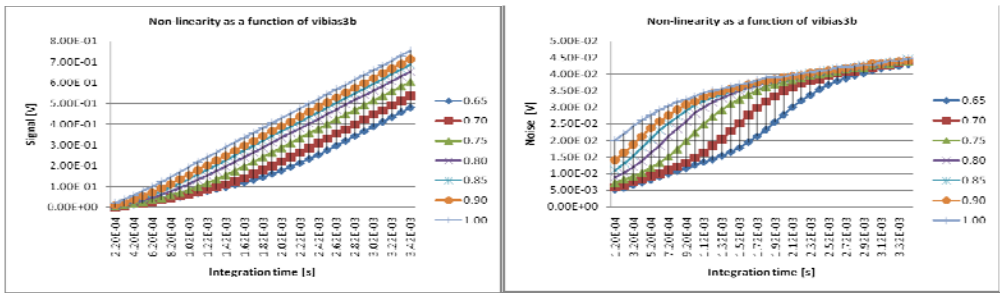

Figure 8 Linearity as a function of the voltage reference of the second stage, vbias3b

6.2 Conversion gain

For the calculation of the conversion gain both cryogenic set-ups have been used with a H-band filter. The transmission curve of the filter is shown in Figure 3. The Conversion gain measurement can be done in several ways, among others with the photometric gain measurement method and with the photon shot noise method. The photometric gain measurement implies the variation of the number of integrated photons on the detector by either varying the integration time or varying the flux of the radiation source (blackbody temperature).

6.2.1 Photometric gain measurement by variation of integration time

The left plot of Figure 9 shows the signal versus integration time at a constant blackbody temperature of 165C

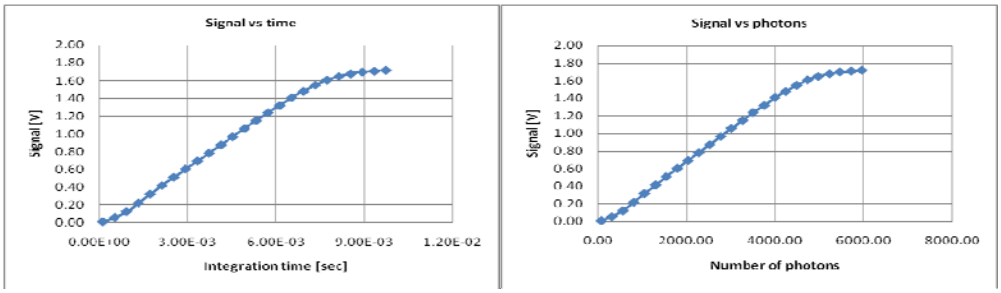

Figure 9 Photometric gain measurement: by variation of the integration time and constant BB temperature of 165 C

The variation of the integration time with a constant blackbody temperature of 165 C yields a conversion gain of 2.68E3 photons/volt. Considering of a QE of 55% we get a gain of:

1.47E3 e^-/volt

6.2.2 Photometric gain measurement by variation of the blackbody temperature

We obtain about the same value for the conversion gain by variation of the blackbody temperature at a fixed integration time. Figure 10 shows the photometric gain measurement with constant integration time of 10 ms and a variation of the blackbody temperature within the range of 65 C to 165 C.

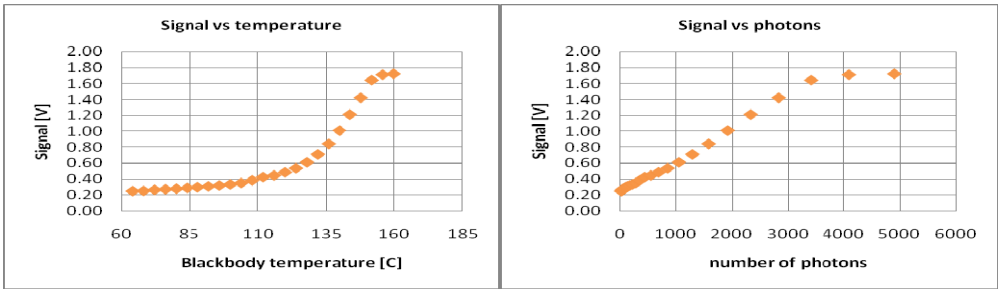

Figure 10 Photometric gain measurement: by of blackbody temperature and constant integration time of 10ms

Calculation of the conversion gain yields a value of 2.49E3 photons /volt. Considering of a QE of 55% we get a gain of:

1.37E3 e^-/volt

6.2.3 Photon shot noise method

The photon shot noise method requires the measurement of the noise-squared, or variance versus the signal as shown in Figure 11. The inverse of the slope of variance versus signal gives the conversion gain [2]. For this measurement the same data as in section 6.2.1 have been used. The plot curve in Figure 11 shows two different slopes. The first part of the curve has a slope of 177 e^-/volt, whereas in the second part we see a slope of 646 e^-/volt. The value derived from the first slope is not useful, but the second slope yields a value which is very close to the design value specified by Teledyne. Why we observe two different slopes is not fully understood and may be caused by some kind of threshold effect. Although the conversion gain obtained from the second part of the curve is very close to the simulated design value of Teledyne we believe that the gain value from the photometric gain measurement is more reliable one. It seems that the readout noise is not shot noise limited over the entire signal range, which is essential for the shot noise method.

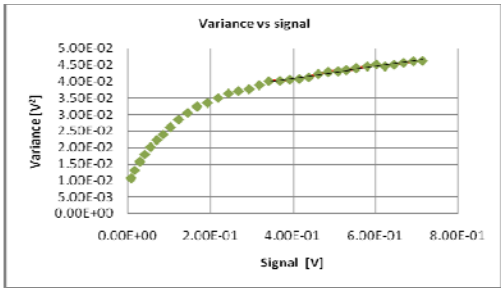

Figure 11 Conversion gain measurement based on photon shot noise method

6.3 Readout Noise

Table 2 shows a summary of both measurement methods in addition to the design value of Teledyne. Whereas the conversion gain with photon shot noise method is very close to the design value, the gain obtained from photometric measurements is two times lower.

method	photometric	shot noise	Data sheet
conv. gain (e^-/volt)	1420	646	769

Table 2 Conversion gain obtained by different measurement methods

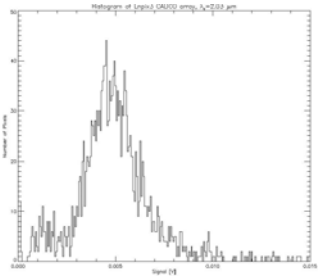

Figure 12 Noise histogram of Lnpix3 with a Vbias3b value of 0.65V

The readout noise measured with the dark detector as a function of Vbias3b is given in Table 3 and his noise histogram is shown in Figure 12. By taking the readout noise from Table 3 and using the conversion gain from Table 2 the readout noise can be calculated in e^- rms. It should be mentioned that all measurements in this paper have been done with a frame rate of 2000 Hz, which is quite high.

Vbias3b (V)	0.65	0.70	0.75	0.80	0.85
readout noise in dark (**V**)	5.13E-03	5.85E-03	7.23E-03	8.77E-03	1.09E-02
Noise: photometric (**e**$^-$)	7.28	8.31	10.27	12.45	15.44
Noise: shot noise (**e**$^-$)	3.31	3.78	4.67	5.67	7.03
Noise: Teledyne (**e**$^-$)	3.94	4.50	5.56	6.74	8.36

Table 3 Readout noise as a function of the voltage reference of the second stage

The system noise and the noise contribution of each stage can be checked separately by switching off one of the stages. The left picture of Figure 13 shows the noise histogram of the first stage and the right picture from the second stage. Total noise values are 780 µV from the first stage and 510 µV from the second stage, which are negligible.

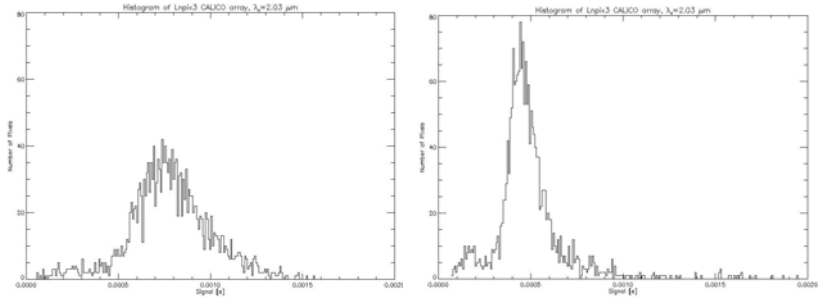

Figure 13 Noise contribution the two CTIA stages. Left: Noise of first stage. Right: Noise of second stage

6.4 Homogeneity

The Lnpix3 structure of the CALICO detector is organized in 16 rows x 128 columns. The picture in Figure 14 was made with the Lnpix3 structure by covering the half of the detector, just at the entrance window outside the camera, and illuminating the other half by a blackbody with a temperature of 165 C. The lower rows of the detector show a higher value (more intensity). This behavior is not understood and further measurements are needed to find out the reason.

Figure 14 showing the homogeneity of the Lnpix3 structure

7. NEXT AO SENSOR, SPEEDSTER

Teledyne has announced the production of the next high speed AO sensor SPEEDSTER, which is the successor of the CALICO detector with the following features:

- Built-in bias and timing
- Digital output (12 bit /40 Msps) in 256x256 version, analog in 128x128 version
- CTIA amplifier with low noise 3-5e^- single read
- Programmable gain CTIA: high gain 320 µV/e^- (0.5 fF), low gain 32 µV/e^-(5 fF).
- Global shutter integrate while read and non-destructive read

The conceptual structure of the speedster is shown in Figure 15.

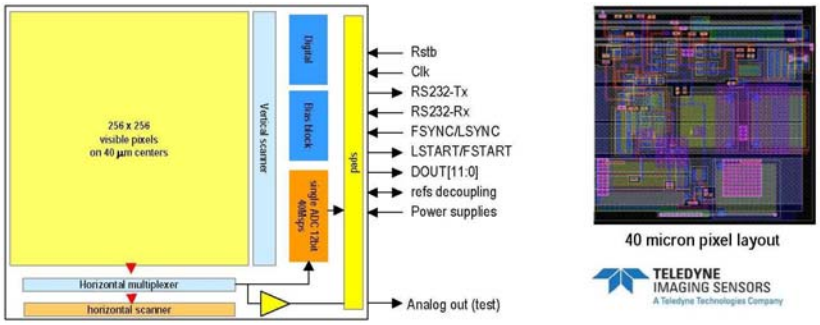

Figure 15 the conceptual structure of the Speedster

The comparison of the Lnpix3 structure (Figure 2) and Speedster (Figure 16) reveals the similarity of both designs. Except for some other improvements like processing and implementation of the cell design the most important change is the reduction of the gain of the second stage. The second stage of the Speedster has a gain of one which reduces the total gain of the Speedster. The Speedster will have a total gain of a quarter of the Lnpix3 (i.e. 320 µV/e^-). This lower gain is based on the experience obtained with the evaluation of the CALICO detector.

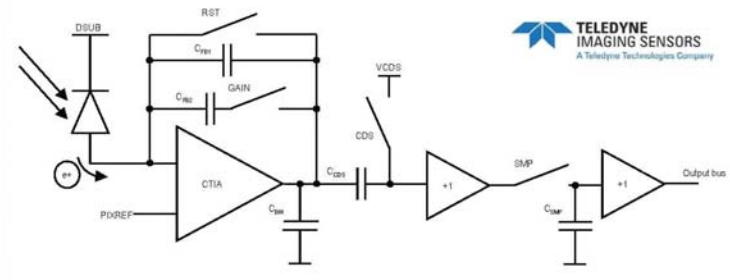

Figure 16 simplified design structure of the Speedster given by Teledyne as proprietary information

8. CONCLUSION AND OUTLOOK

Low readout noise at high readout speed is accomplished by high gain and signal processing circuitry under each pixel. Tests show that the Lnpix3 structure works well after optimizing the bias voltage setting within a narrow range. The main reason for the development of the CALICO detector was the selection of the best design and using it as a platform for the next AO sensors. SPEEDSTER will be the successor of the CALICO based on the Lnpix3 design which will be tested at ESO once it becomes available.

9. ACKNOWLEDGMENTS

Obviously the evaluation of the CALICO detector could not be successful without the help and support of the development team of Teledyne Imagine Sensors. We would like specially to thank Anzhelika Kononenko, Atul Joshi, and John C. Stevens for their great support.

10. REFERENCES

[1] Atul Joshi, John Stevens, Anzhelika Kononenko, and John Blackwell, Teledyne (Rockwell) Scientific, 5212 Verdugo Way, Camarillo, CA, USA 93012

[2] Finger G., Dorn R., Meyer M., Mehrgan L., Moorwood A.F.M., and Stegmeier J., "Interpixel capacitance in large format CMOS hybrid arrays", Proc. SPIE Vol. 6276, 62760F (2006).

[3] Finger, G., R. Smith, S. Menardi, R.J Dorn, M. Meyer, L. Mehrgan, J. Stegmeier, A.F.M. Moorwood, (2004), Performance limitations of small format high speed infrared arrays for active control loops in interferometry and adaptive optics.

[4] Meyer, M., Finger, G., Mehrgan, H., Moorwood, A. F. M., Stegmeier, J. (1996), The ESO Infrared Detector High-Speed Array Control and Processing Electronics IRACE, In: The ESO messenger 86, pp.14-17