WE MUST BE MAD

Pushing FIERA to its Limits

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Abstract: *MAD (<u>M</u>ulti conjugate <u>A</u>daptive optics <u>D</u>emonstrator) is an MCAO pathfinder experiment for both OverWhelmingly Large (OWL) 100-m class telescopes and ESO VLT 2nd generation instrumentation. MAD's Wave Front Sensor (WFS) employs five thermo-electrically cooled e2v CCD39-01 devices operating in two modes: The Multi Shack-Hartmann (SH) WFS consists of three CCDs with 80x80 pixels each which are read in parallel at up to 400 frames per second delivering a pixel rate of 4.8 Mpix/sec at lowest noise. The Layer Oriented (LO) WFS is made up with two CCDs of the same type but both detectors are read simultaneously with different frame rates and binning factors using a single FIERA controller. The paper shows the concept of both the SH and LO wave front sensors and gives first performance results from laboratory tests. We report on tricks used to implement and speed up the clock patterns and the lessons learned during the development phase.*

Key words: Adaptive optics; CCD; multi conjugate; Shack-Hartmann; thermo-electrical cooling; wavefront sensor.

1. OVERVIEW

MAD shall investigate two different approaches of MCAO correction with two independent techniques: the Star Oriented MCAO with a Multi Shack-Hartmann Wavefront Sensor (SHWFS) and the Layer Oriented MCAO with a Layer Oriented Wavefront Sensor (LOWFS). The design of the MUSE WFS was driven by the requirement to re-use as many key components (i.e. FIERA) as possible. The design is simplified by the fact that FIERA (Gerdes, 1998) has to operate in only one WFS mode at a time.

The detector system is based on five CCD39-01 devices from e2v technologies. These devices have a split frame transfer architecture with 80x80 active pixels and four outputs and are available in a hermetically sealed package which includes a thermo-electrical (Peltier) cooler.

The hardware configuration for both operating modes of FIERA is shown in Table 1. Each video board has four channels, each clock board can provide 14 fully programmable clocks (only 10 are used for MAD) and the bias board can provide a total of 32 DC voltages to the CCD chips.

Table 1. FIERA configuration for MAD

Item	SHWFS	LOWFS
Bias board	CCD1, 2, 3	CCD4, 5
Clock driver I	CCD1	CCD4
Clock driver II	CCD2	CCD5
Clock driver III	CCD3	Not used
Video board I	CCD1	CCD4
Video board II	CCD2	CCD5
Video board III	CCD3	Not used
Communications board	Required	Required

2. SHACK-HARTMANN WAVEFRONT SENSOR MODE (SHWFS)

As can be seen from Figure 1 the timing for the three CCDs is straightforward. All three CCDs are operating with the same frame rate and binning factors (1x1 or 2x2). In principle, the three CCDs could be operated by only one clock driver board because the timing is absolutely identical. However, it turned out that the wiring gets more complex and the performance is reduced due to longer cable lengths and larger capacities. Therefore each CCD is now driven by its own clock driver board which also makes chip specific settings of clock levels possible.

The frame rate required for the SHWFS mode is 400 Hz (for a 64x64 window). Given the constraints from the CCD39-01 datasheet for maximum vertical and horizontal clocking rates and from FIERA for the maximum pixel rate that can be handled a timing budget was established. Table 2 shows this budget, assuming four horizontal prescan, one “pipeline” and two overscan pixels (to clean the horizontal register) per CCD quadrant. Similarly two overscan lines for each half of the CCD are factored in.

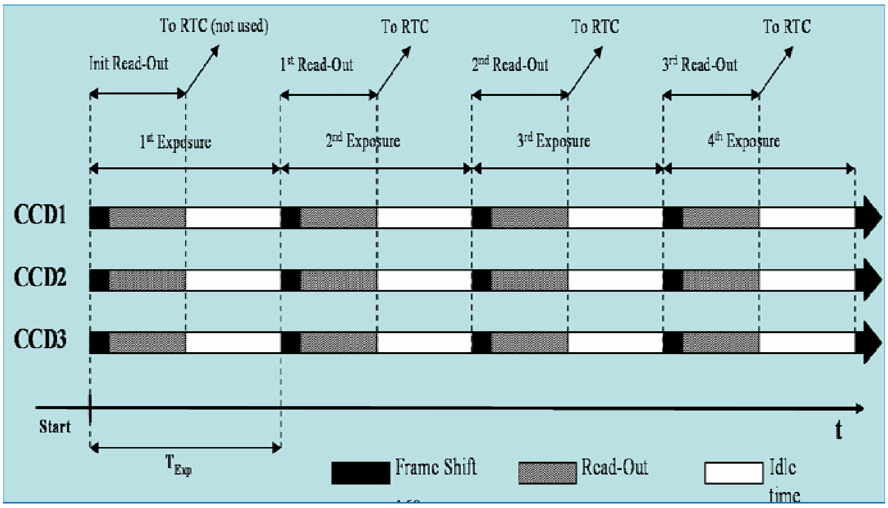

Figure 1. Shack-Hartmann readout sequence

Table 2. Timing budget for SHWFS and LOWFS modes

Chip format	
No. of outputs hor.	2
No. of outputs ver.	2
Total hor. pixels	94
Total ver. pixels	84

Mode	**SHWFS 1x1**	**SHWFS 1x1 windowed**	**LOWFS 2x2**	**LOWFS 4x4**
No. active hor. pixels	94	64	94	94
No. active ver. pixels	84	64	84	84
Binning hor.	1	1	2	4
Binning ver.	1	1	2	4
No. active pixels	7896	4096	7896	7896
Inactive hor. pixels	0	1920	0	0
Inactive ver. lines	0	20	0	0
System timing	**µs**	**µs**	**µs**	**µs**
Pixel period	1,60	1,60	1,60	1,60
Horizontal shift	0,60	0,60	0,60	0,60
Vertical shift	2,00	2,00	2,00	2,00
Results	**µs**	**µs**	**µs**	**µs**

Frame transfer	84,00	84,00	84,00	84,00
Clear line	56,40	56,40	56,40	56,40
Read active pixels	3158,40	1638,40	789,60	197,40
Binning overhead	0,00	0,00	296,10	222,08
Skip inactive pixels	0,00	288,00	0,00	0,00
Skip lines	0,00	20,00	0,00	0,00
FIERA overhead	n/a	600,00	n/a	n/a
Frame period	3298,80	2686,80	1226,10	559,88
Max. frame rate [Hz]	303,14	372,19	815,59	1786,11

Unfortunately FIERA created unexpected overheads in executing the CCD clock patterns which slowed down the frame rate in SHWFS windowed mode from theoretically possible 480 Hz to a much lower value of approx. 370 Hz. One kind of overhead was identified in the execution of loops, another was observed when executing very short clock patterns (i.e. vertical line shift with 2 µs duration, but approx. 9 µs overhead). The loop overhead was reduced by unrolling the inner loops of the timing patterns which are executed 32 times in the case of windowed SHWFS mode. The second measure taken was to combine the short patterns for line shifting and skipping pre- and overscan pixels into one single pattern. After these modifications the “execution” time of 4000 frames has been measured to be 10.2 s which corresponds to a frame rate slightly below 400 Hz.

3. LAYER ORIENTED WFS (LOWFS)

The timing for the LOWFS mode is more complex (Figure 2). Not only are the two CCDs read with different frame rates (1:2 or 1:4) but both CCDs require different binning factors. FIERA makes use of local microsequencers on each clock and video board. These microsequencers are loaded, triggered and monitored by the DSP controlling the complete readout sequence, allowing each board to have a different timing. The only constraint is that the lengths of these clock patterns must be identical.

The issue of the different horizontal binning factors for the two CCDs was addressed by a clock pattern that bins four pixels on one CCD but only two pixels on the other, by omitting clock transitions on the latter. As the standard FIERA software expects equal numbers of pixels read from all CCDs dummy pixels are read from the CCD with the higher binning factor. They are ignored by the subsequent image processing routines. A similar method is applied for the vertical binning. While the first CCD is subject to four line shifts two of them are skipped on the second device.

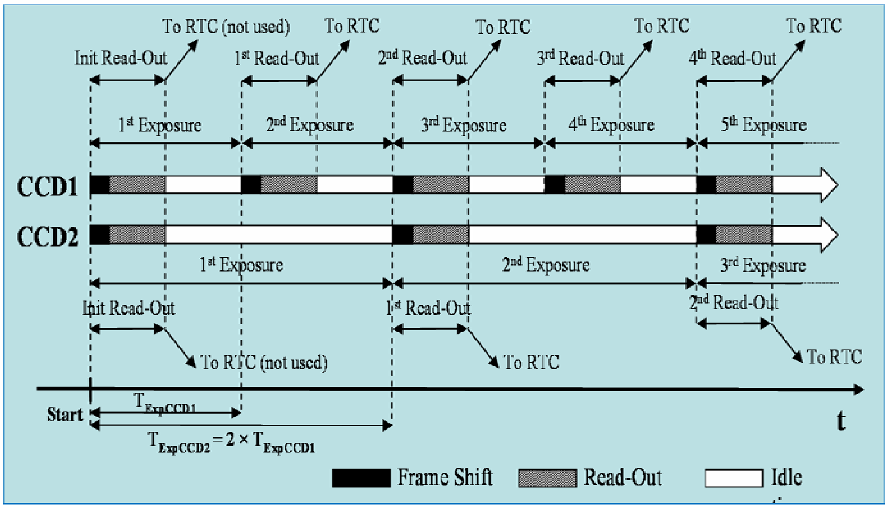

Figure 2. Layer oriented readout sequence

The different frame rates are done in such a way that a virtual frame is defined which contains two or four frames, depending on the frame ratio of 1:2 or 1:4. While each frame of the CCD with the higher rate is “clocked”, the CCD with the lower rate skips one out of two or three out of four. The result is a frame with many dummy pixels which are ignored by the software.

4. MECHANICAL CONSTRAINTS

The size of the complete detector head is limited to a volume of 96x68x30 mm^3. The electrical connections have to be very flexible because the heads are mounted on motorized x-y-tables. The adopted solution is a rigid-flex printed circuit board (PCB) which contains clock filters, junction FET buffers and constant current loads for each CCD output (Figure 3). The e2v Peltier package is tightly attached by screws to the aluminum base plate. The base plate has mating connectors for water cooling. With an electrical power of eight Watts a temperature difference between hot and cold surface of about 45 °C was measured. With a coolant liquid temperature of typically 10 °C a CCD temperature of -35 °C can be reached.

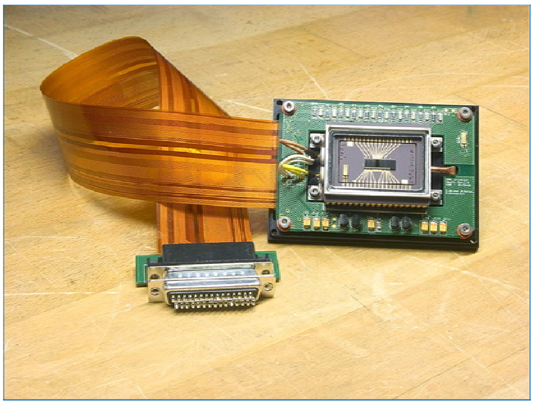

Figure 3. Rigid-flex PCB

5. PERFORMANCE DATA (SHWFS)

Figure 4 shows a typical example of a SHWFS image with three CCDs being read out simultaneously. A frame rate of 400 Hz at 64x192 pixels in total was achieved. This corresponds to an average pixel rate of 4.9 Mpixel/sec and a burst pixel rate of 7.5 Mpixel/sec. The noise level for all 12 channels is approx. 6 e^- RMS, with a conversion factor of 1.7 e^-/ADU.

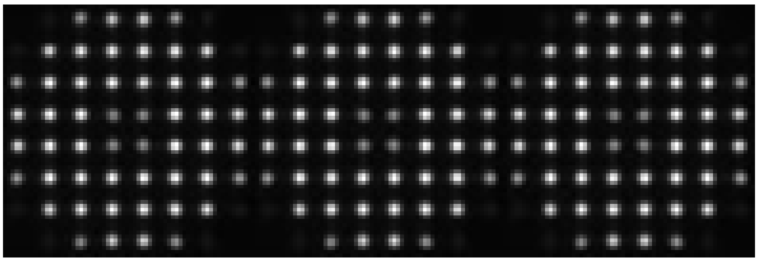

Figure 4. Sample image, Shack-Hartmann mode, 3x64x64 pixels

REFERENCES

Gerdes, R, Beletic J. W., and Duvarney, R. C., 1998, Design concepts for a fast-readout low-noise CCD controller, Proc. SPIE Vol. 3355, Optical Astronomical Instrumentation, ed. Sandro D'Odorico; p. 520-528.