International Image Sensor Workshop, Norway Wrap up

Olaf :

Commercial CMOS situation, links to scientific CMOS, some CCDs, glance at other applications

Mark:

Selected examples of up-coming CMOS technology

>> Details in copies of presentations

Why was this workshop important for us ? (1)

- CMOS detectors are currently undergoing a similar development than CCDs did many years ago
- Development from commercial CMOS to scientific CMOS
  (e.g. E-ELT wavefront sensor development)
- mass market <> specialized market (Goliath <> David)
- It mainly focused on commercial applications in which some of the technologies we require are being industrialized now
- Since we get mostly 2nd hand information from the detector manufacturers (who are exclusively dealing with foundries for the production), it was hard for us to judge how fast e.g. the backside illumination technology or the 3D stacking process will be available as a standard process in the future
- It brought together manufacturers, detector designers, foundries, as well as the symposium on backside thinning (one key technology)

Why was this workshop important for us ? (2)

- Getting to know the key players:
  - **Research:** JPL Fossum (then founder of various companies), Wadsworth, Pain, Janesick (now Sarnoff), Lesser (thinning)
  - **CMOS design:** IMEC, Fill factory, Cypress, Caeleste, CMOSIS, Alexima
  - **Foundry:** Tower, TSMC, UMC, Jazz
  - **Manufacturers:** Sony, Photobit, Micron, Aptina, Siimpel, Dalsa,
  - **Commercial Thinning:** Omnivision, ST (former Thomson)

- In addition many useful informal discussions for curved CCD development, largest format monolithic CCD detectors, L3 technology and latest CMOS developments

The paradox: Why more is less

Electronic consumer device with largest turn-over and highest marketshare: Cell phones >> Cell phone CMOS imagers

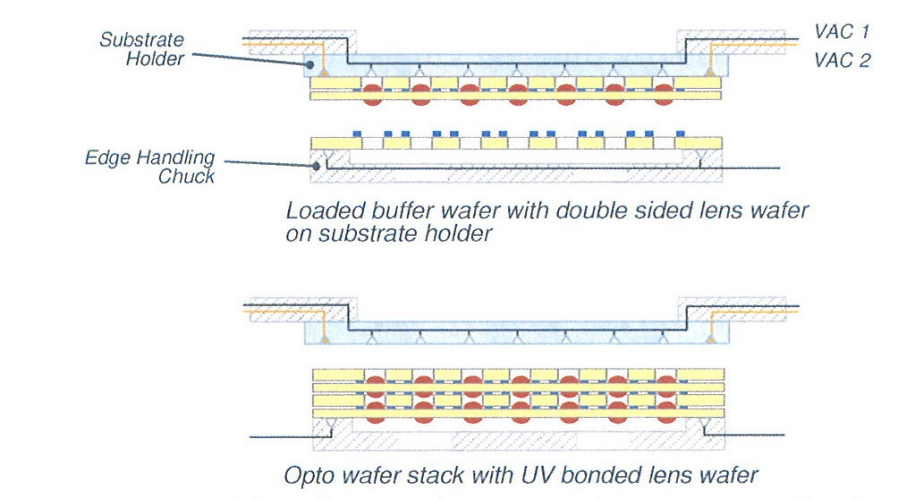
Image quality is **not** the driving parameter, **but** the megapixel race for marketing reasons (quantity not quaility) – size of imager itself stays constant or shrinks

In principle a low quality consumer product (overall) with partially amazing CMOS performance for some parameters, e.g. < 1e- D.C. at room temperature, 2 e- RON, full integration

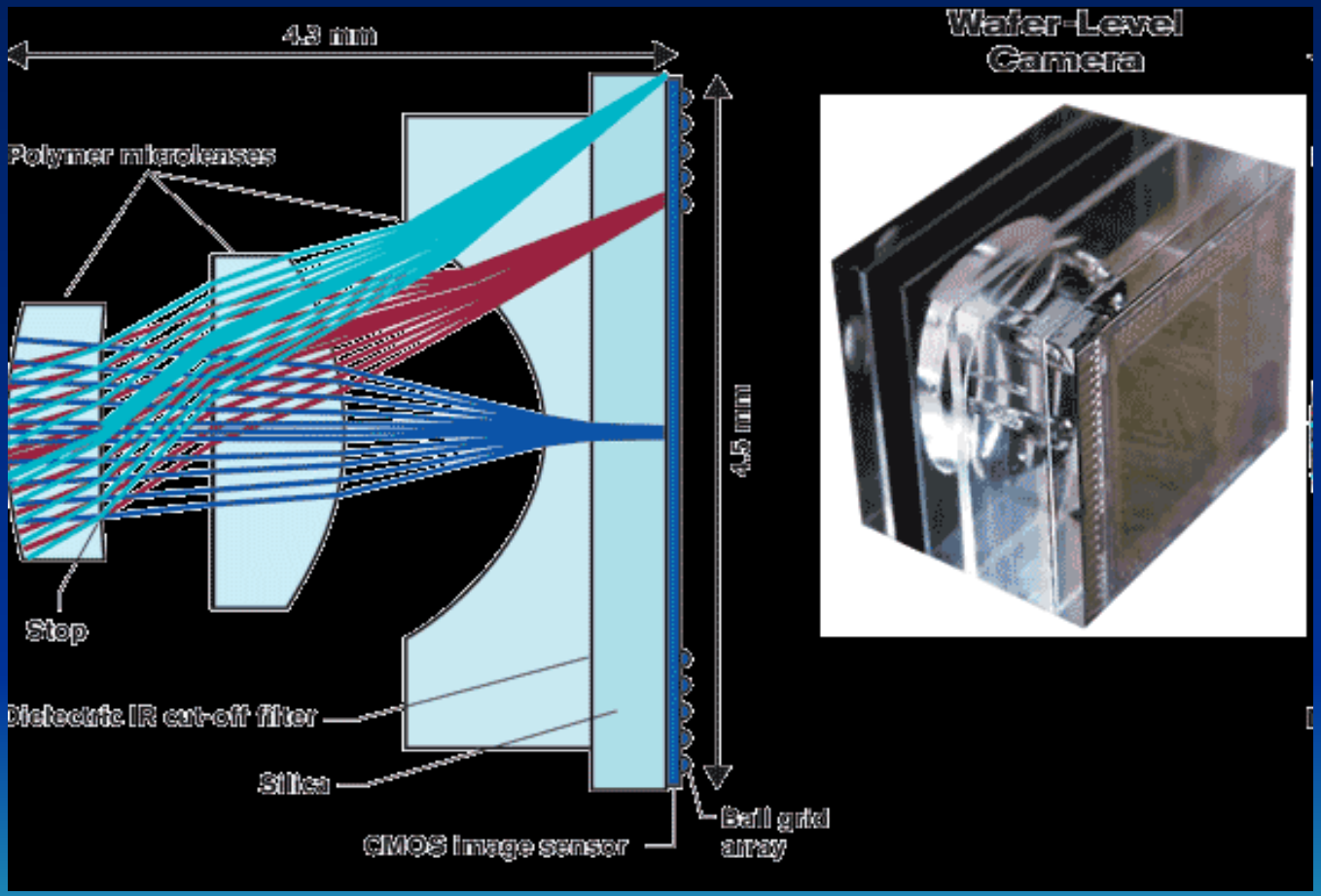
Main needs are smaller pixels (standard 1.4 um), as of marketing and need for smaller camera module, and more waferscale integration of wafer processed optics > wafer level camera (see also www.suss.com & www.aptina.com)

(Subjective performance measurements due to 'pretty' pictures)

The paradox: Why more is less



The paradox: Why more is less



Cell phone market

Around 1.04 billion cell phones will be sold in 2009 (research group Gartner)

- The Asia Pacific region is seen as becoming even more important, with one out of every three mobile phones sold in the area in 2009.
- “China and India alone will account for nearly 200 million units in 2007, with the Indian market surpassing China in 2009 to reach 139 million units,” Asia Pacific analyst Ann Liang.
- Vendors including Finland’s Nokia, US-based Motorola and Samsung Electronics from South Korea will generate combined revenues of $1.7 billion in 2009.
- The average price per cell phone will slip to $161 in 2009 from $174 in 2004, the study said, even though the handsets will have more memory and better screens and cameras than current models.

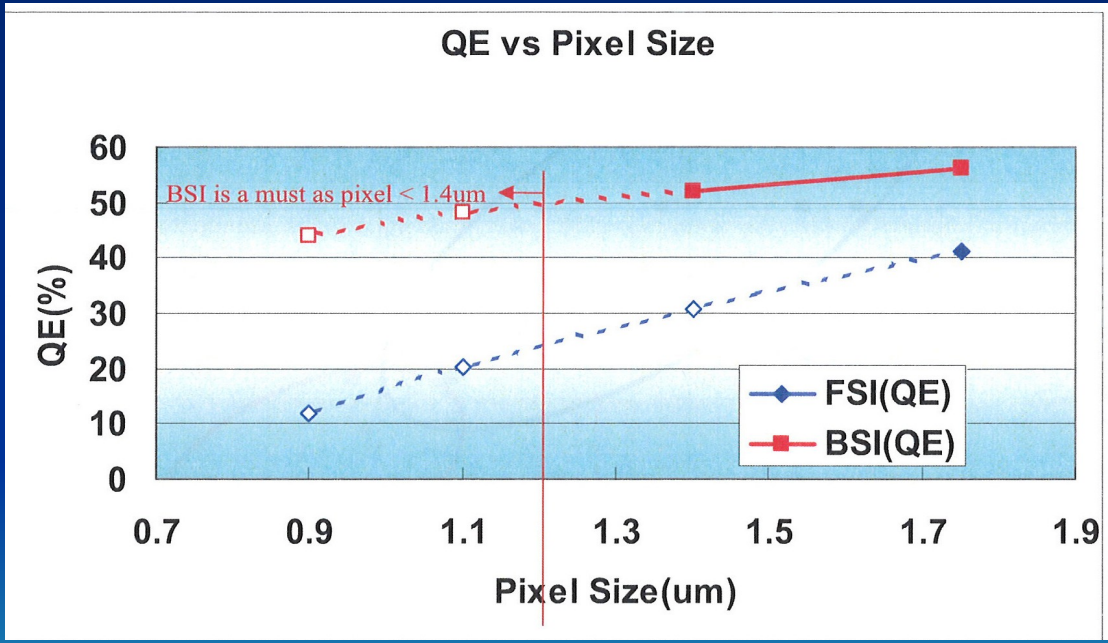
An idea of the size and integration:

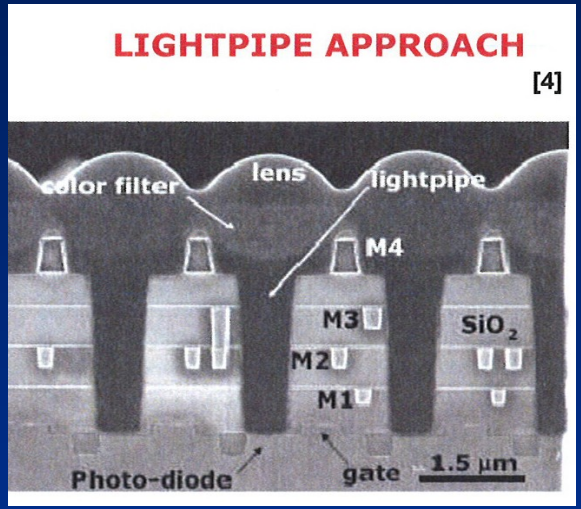
- CMOS imager (rolling shutter)
- All readout electronics on same chip
- Beyer color filter
- Microlens array
- Optics

Backside illumination

- Why backside thinning for those cell phones ?
- Different backside thinning technologies
  - Bulk versus SOI thinning technology
- Different surface treatments
  - Chemisorption, laser anneal, MBE, SOI integrated technique

Backside illumination

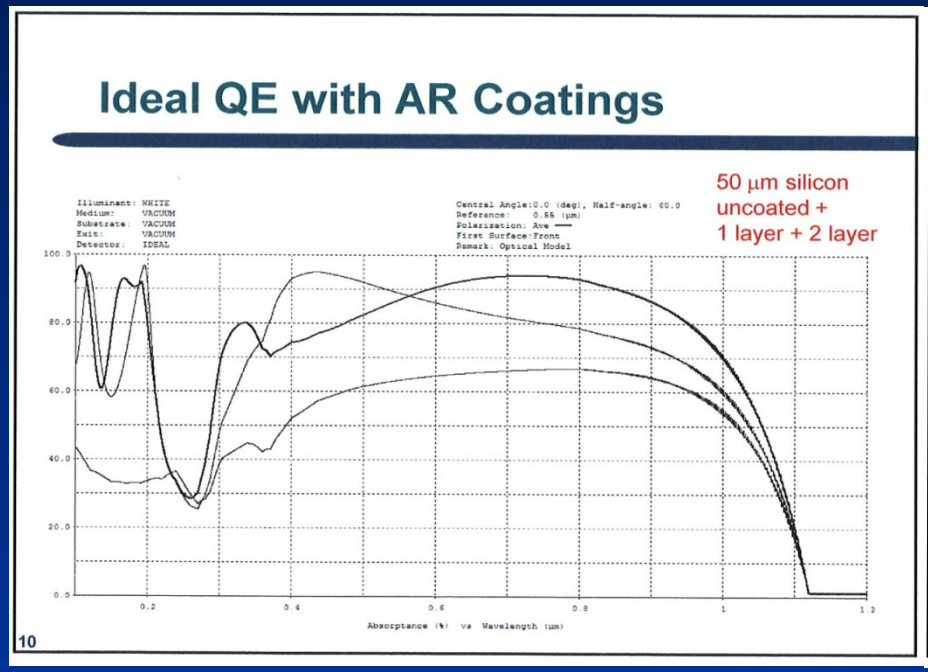


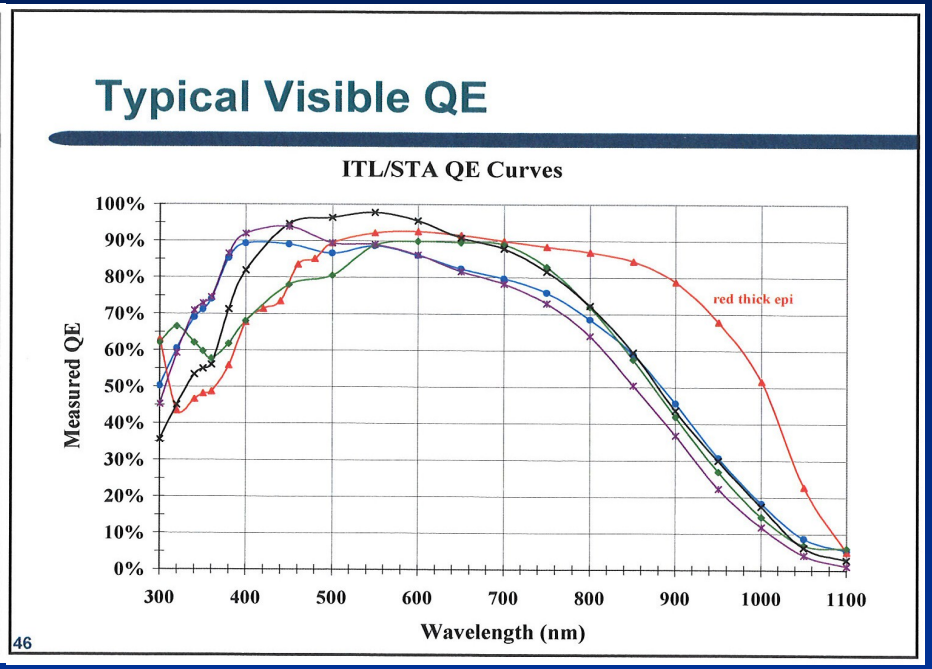


Thinning R&D 1
Mike Lesser (CMOS) thinning

- Bulk thinning (backside grind, hybridize with silicon substrate, epoxy underflow, acid etching, chemisorption, AR coat, package)
- (Standard CCD product now STA0500 A, 4kx4k, 15um CCD)
- No principal problem to thin CMOS similar to CCDs, BUT general trend that thinning increases RON (1 e-) and defects

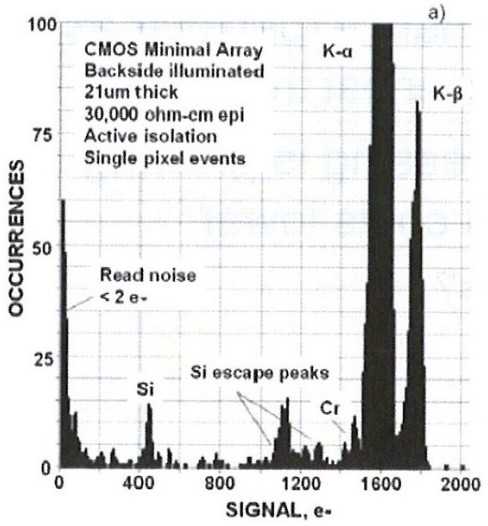
Thinning R&D 1
Mike Lesser (CMOS) thinning

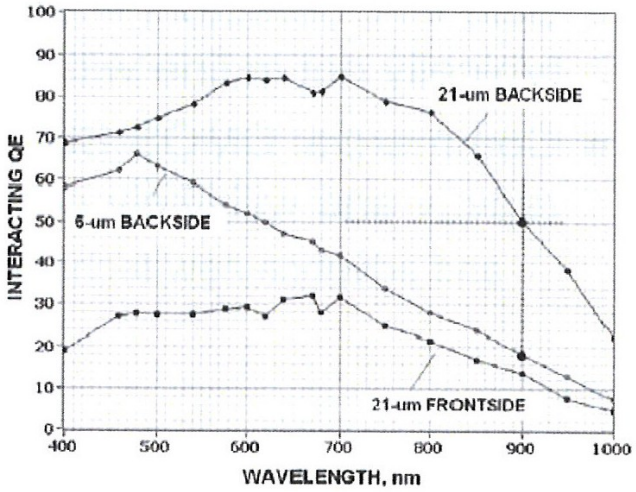




Thinning R&D 1
Mike Lesser (CMOS) thinning

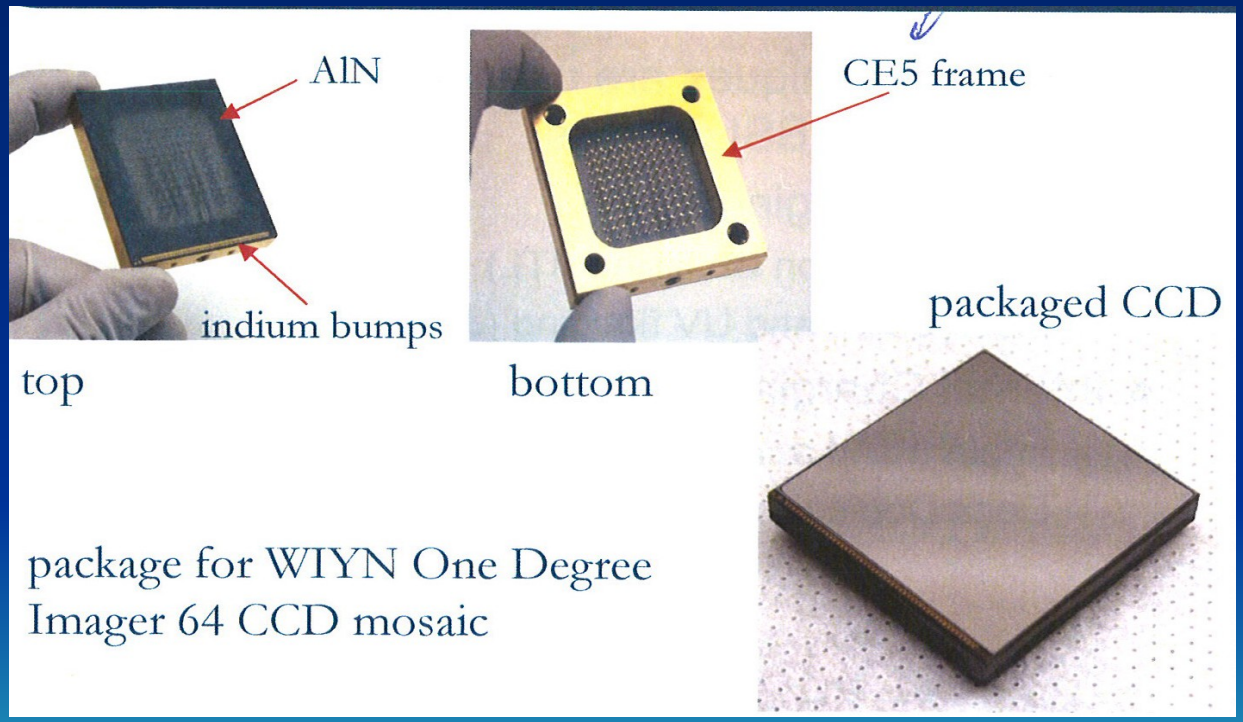
BSI CMOS – Sarnoff/ITL





Lesser thinned CCDs Orthogonal Transfer Arrays

- Four side buttable STA2200A



Thinning (Semi) R&D 2
Demand for backside illuminated, thinned (75-250 um) fully depleted CCDs as seen by LBNL

—Subaru Super and HyperSuprime Cameras

- 10, 2048 x 4096 (15 μm pixel), 200 μm thick, fully depleted p-channel CCDs in operation since August 2008 (Super Suprime-Cam)
  - —http://www.naoj.org/Pressrelease/index_2008.html#081120
- HyperSuprime-Cam will require ~ 200 CCDs
- Fabricated by Hamamatsu Corporation

Thinning (Semi) R&D 2
Demand for backside illuminated, thinned (75-250 um) fully depleted CCDs as seen by LBNL

—Pan-Starrs (University of Hawaii)

- 1.4 Gpixel camera, 1 installed August 2007 with 3 more proposed
- MIT Lincoln Laboratory orthogonal transfer, 75 μm thick fully depleted n-channel CCDs fabricated on ~ 5 kΩ-cm, p-type silicon
- 60, ~ 5k x 5k (10 μm pixel) CCDs per camera
- http://pan-starrs.ifa.hawaii.edu/public/
- Similar project: WIYN Observatory One-degree imager

Thinning (Semi) R&D 2
Demand for backside illuminated, thinned (75-250 um) fully depleted CCDs as seen by LBNL

—Dark Energy Survey camera

- 62, 2048 x 4096 (15 μm pixel), 250 μm thick, fully depleted p-channel CCDs (~ 0.5 Gigapixel camera)
- Fabrication at DALSA/Lawrence Berkeley National Laboratory, packaging and testing at Fermi National Accelerator Laboratory
- http://www.darkenergysurvey.org/

—Large Synoptic Survey Telescope (LSST)

- ~ 200, 4k x 4k (10 μm pixel), 100 μm thick, fully depleted CCDs required (~ 3.2 Gigapixel camera)
- http://www.lsst.org/lsst/science/concept_camera

Thinning (Semi) R&D 2
Demand for backside illuminated, thinned (75-250 um) fully depleted CCDs as seen by LBNL

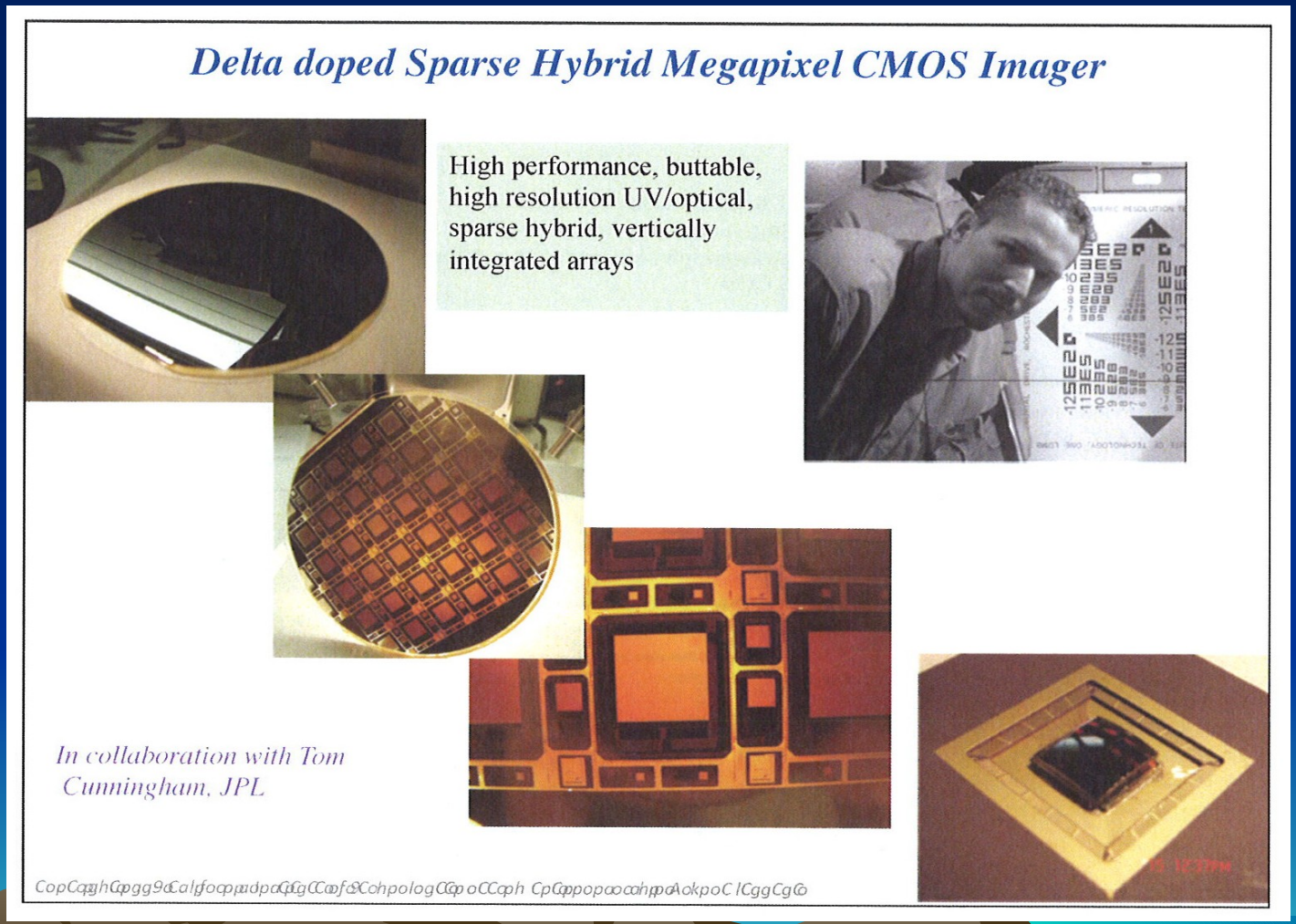
- Hybrid approach Dalsa fabbing 80%, commercial thinning step, last processing steps of thinned material at LBNL
- 4k x 4k ,15 um now fabricated at LBNL, for Sloan > SDSS III (sample device, clean test images shown, RON 2.9 – 4 e-, DC 0.7 e-/pix hour at -140 C) , page 78

Backside treatment R&D 1
JPL Delta doping (MBE)

- Not done in industry
- Invented at JPL in late 80s, now available also to other customers and rated to be the most stable process of backside treatment (surface passivation)

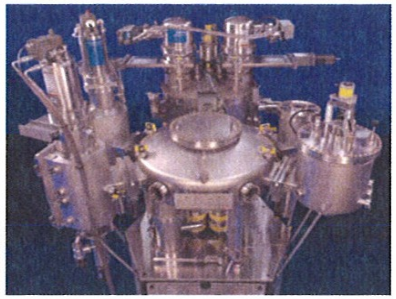
((Curved FPA's))

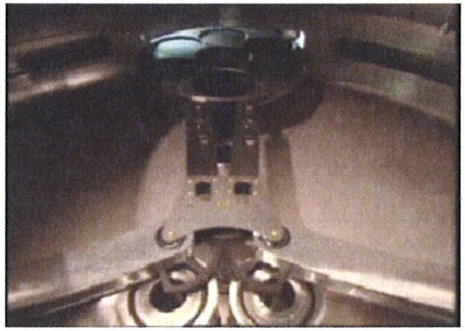
Backside treatment R&D 1
JPL Delta doping (MBE)

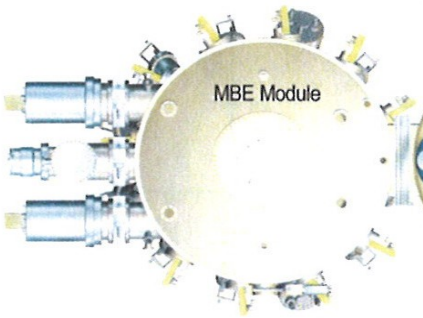


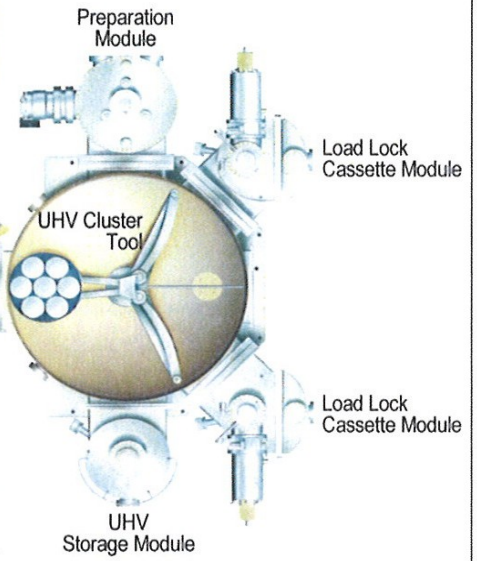
Backside treatment R&D 1
JPL Delta doping (MBE)

8-inch Wafer Silicon MBE



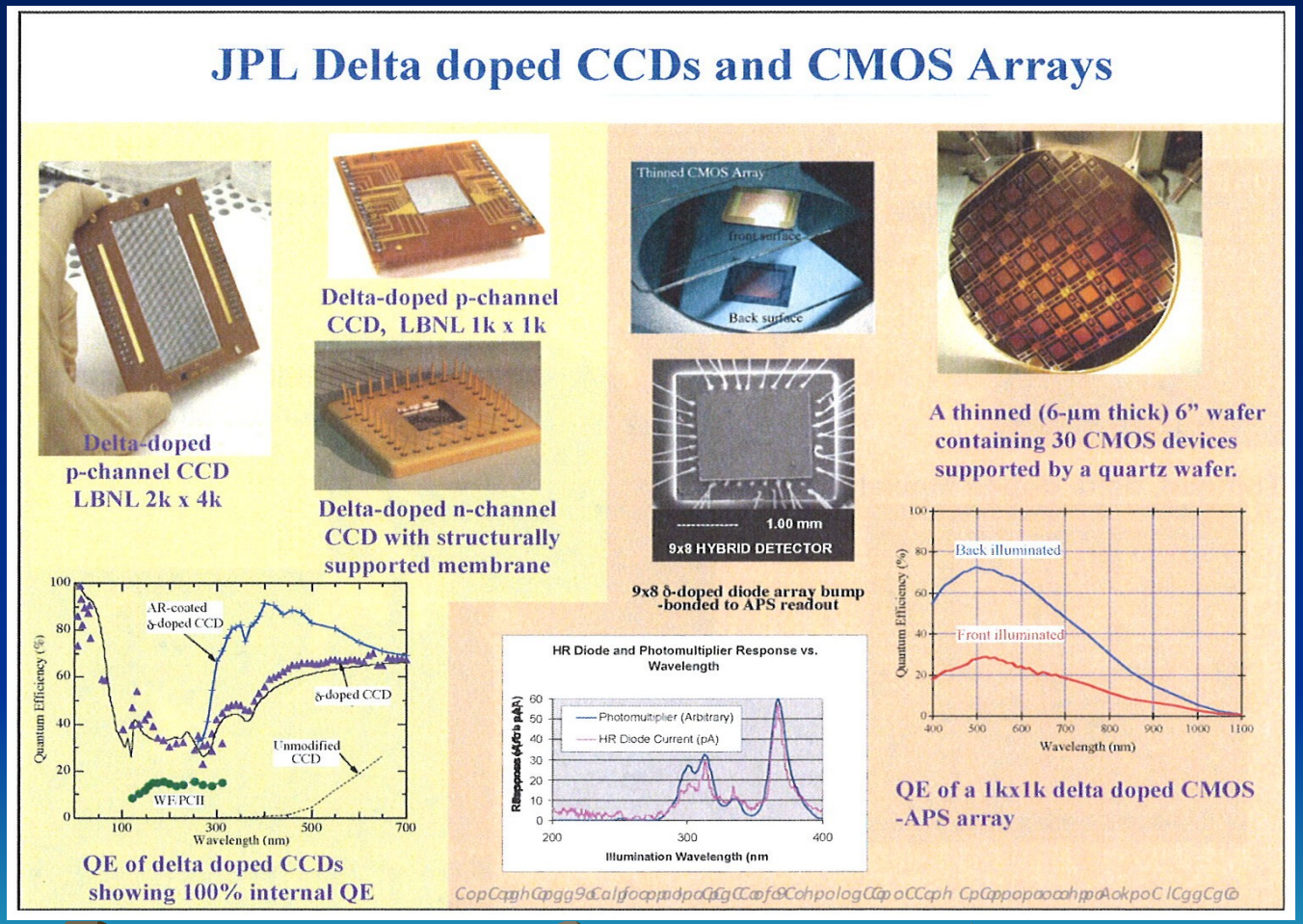






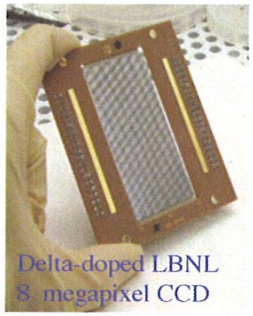
With large size wafer capacity and multiple wafer processing, high throughput processes is enabled and delta doping a lot run can be achieved in short period of time

Backside treatment R&D 1
JPL Delta doping (MBE)

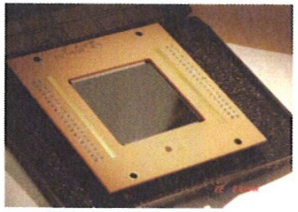


Backside treatment R&D 1
JPL Delta doping (MBE)

Delta doped Large Format P channel CCDs

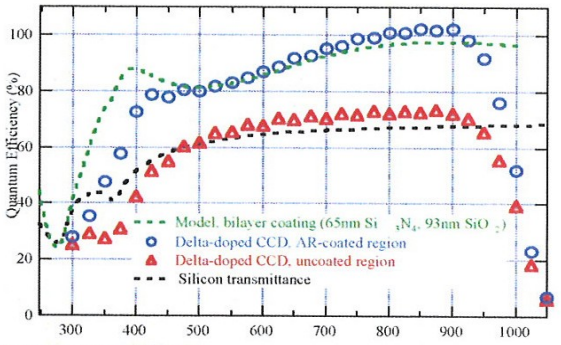


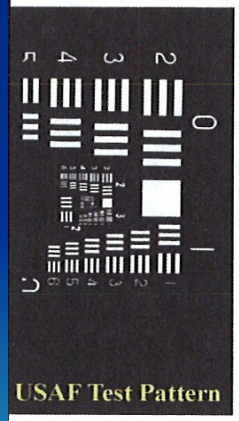
Delta-doped LBNL
8 megapixel CCD



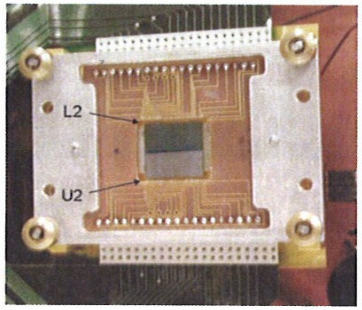
Delta-doped LBNL
10 megapixel CCD

MBE Growth on P-channel High Purity CCDs





USAF Test Pattern



Collaboration with Steve Holland, Chris Bebek, Natalie Roe, Lawrence Berkeley National Laboratory

Dark current ~ 1 e-/pixel/hr

Commercial Thinning (1)
TSMC profile

- TSMC is the world's largest dedicated semiconductor foundry providing the industry's leading process technology, library and IP options and other leading-edge foundry services. TSMC operates a six-inch wafer fab, five eight-inch wafer fabs and two 12-inch wafer GigaFabs.
- In 2006, total capacity at TSMC exceeds seven million 8-inch equivalent wafers.

Commercial Thinning (2)

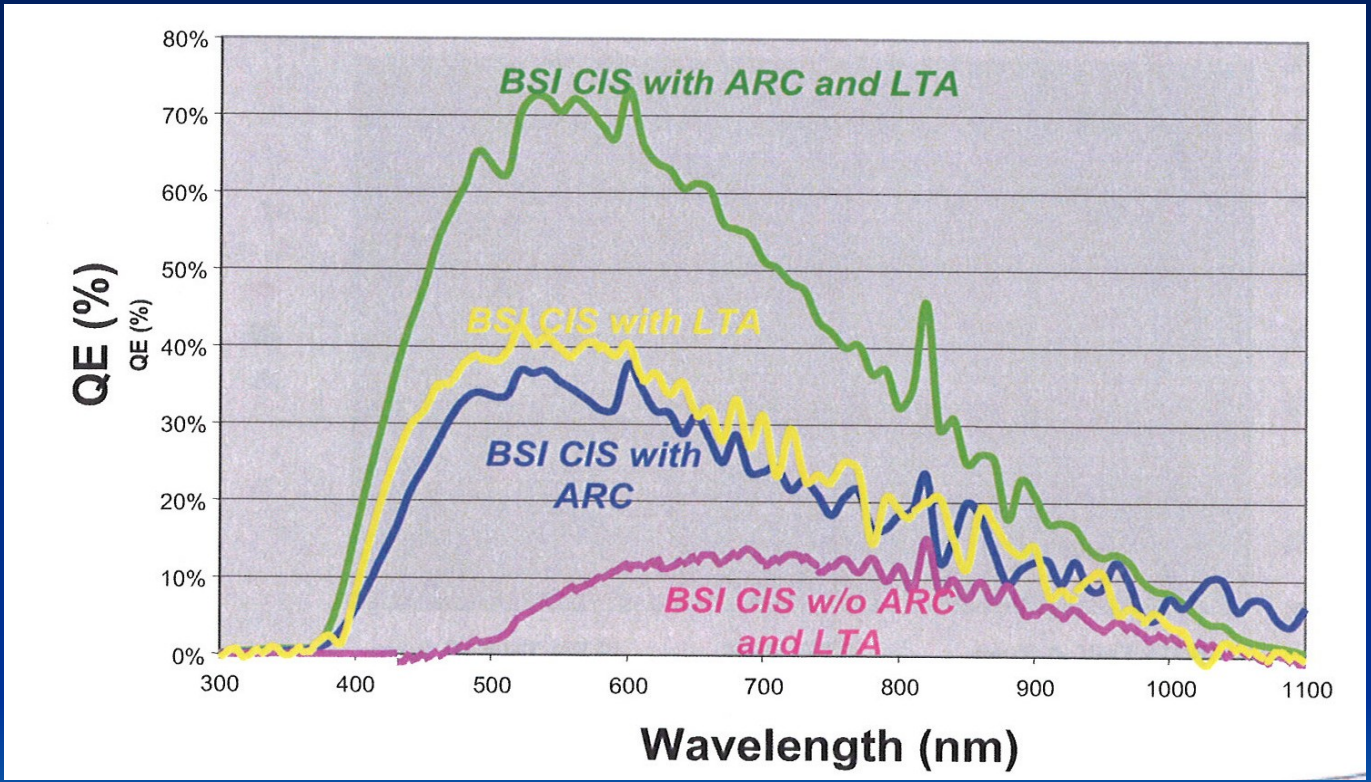
The good news:

- Omnivision (455 million camera chips / year) & TSMC is the first partnership to provide backside illuminated CMOS to mass production since early this year (5 year development)
- The approach was to base this development onto existing technology (bulk Si thinning / laser anneal), which might be more costly, but earlier on the market than SOI
- Gapless microlenses, with different heigth pattern for focussing capability and improved color perfromance (thickness variation)
- Achieved same yield than frontside devices
- Full well 5000 e- with 1.4. um pixel

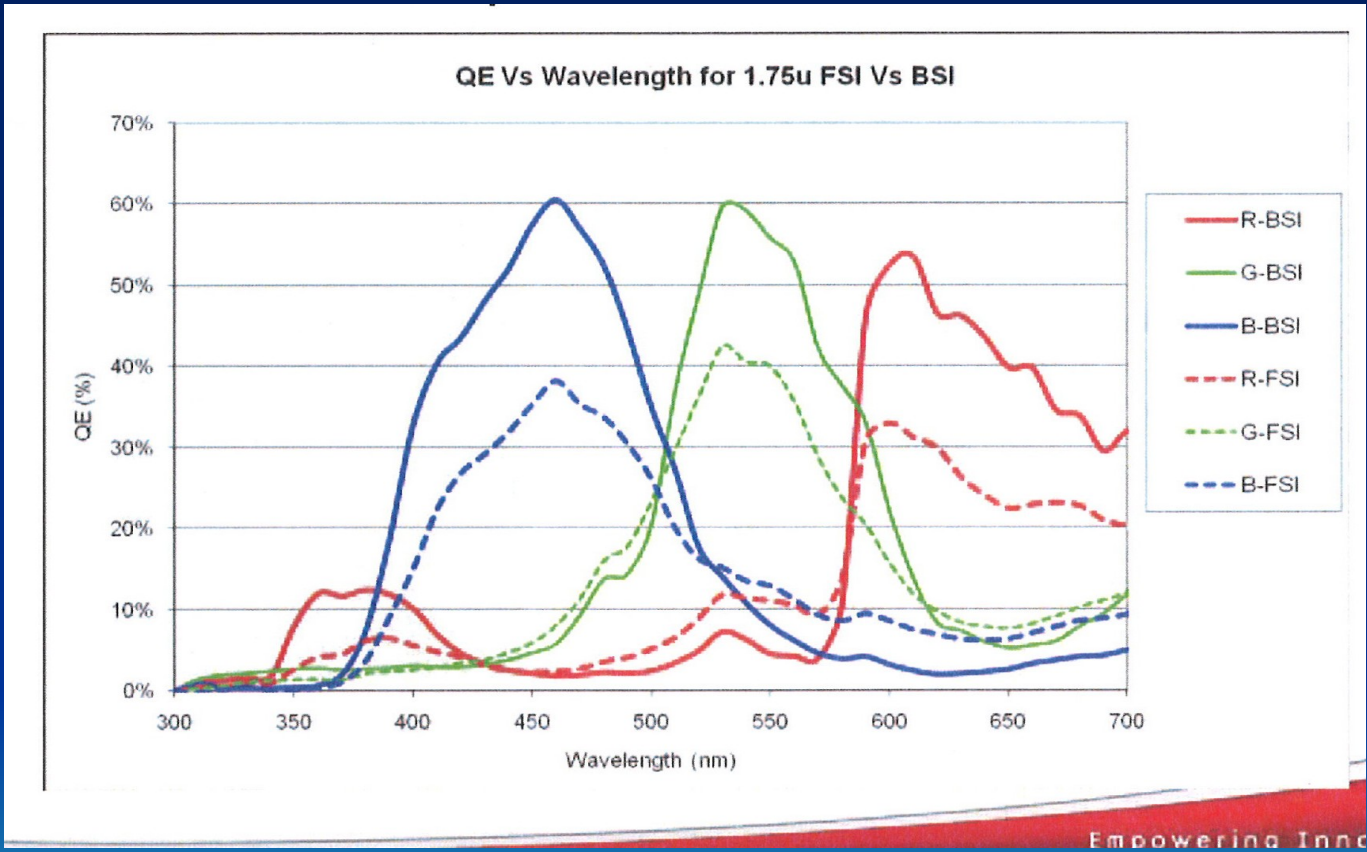
The bad news:

- In the next couple of years this technology is not available to normal customers.
- No interest in providing small quantities for scientific imaging

Commercial Thinning (2)



Commercial Thinning (2)



Commercial Thinning (3)

ST is following more the path of SOI thinning

- (Bulk process looks to be a less robust process to them)

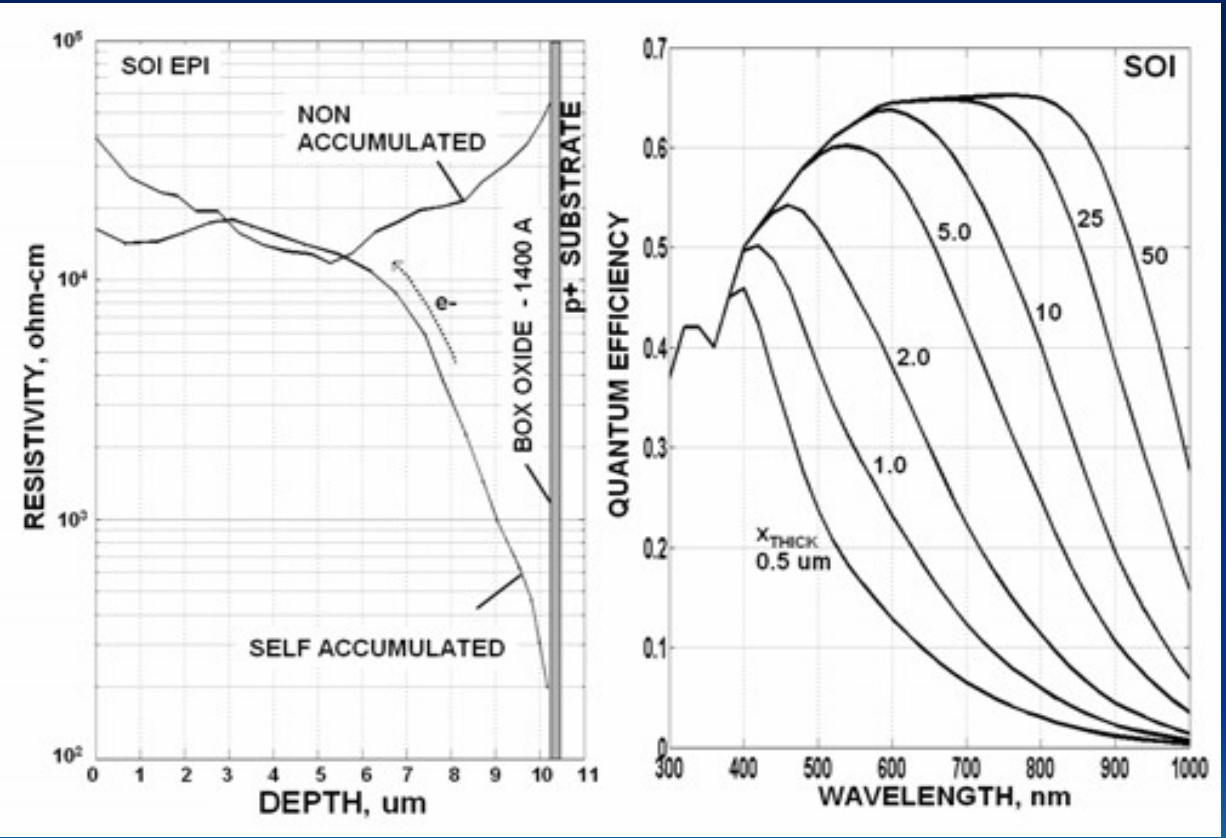
Advantages SOI: Easier to process

- Self accumulated SOI (developed by Sarnoff) makes thinning easy for visible applications through ‘automatic’ etch stop at the oxide layer
- At the same time the oxide layer acts as surface passivation and AR coating opposed to separate process steps (MBE, AR..)

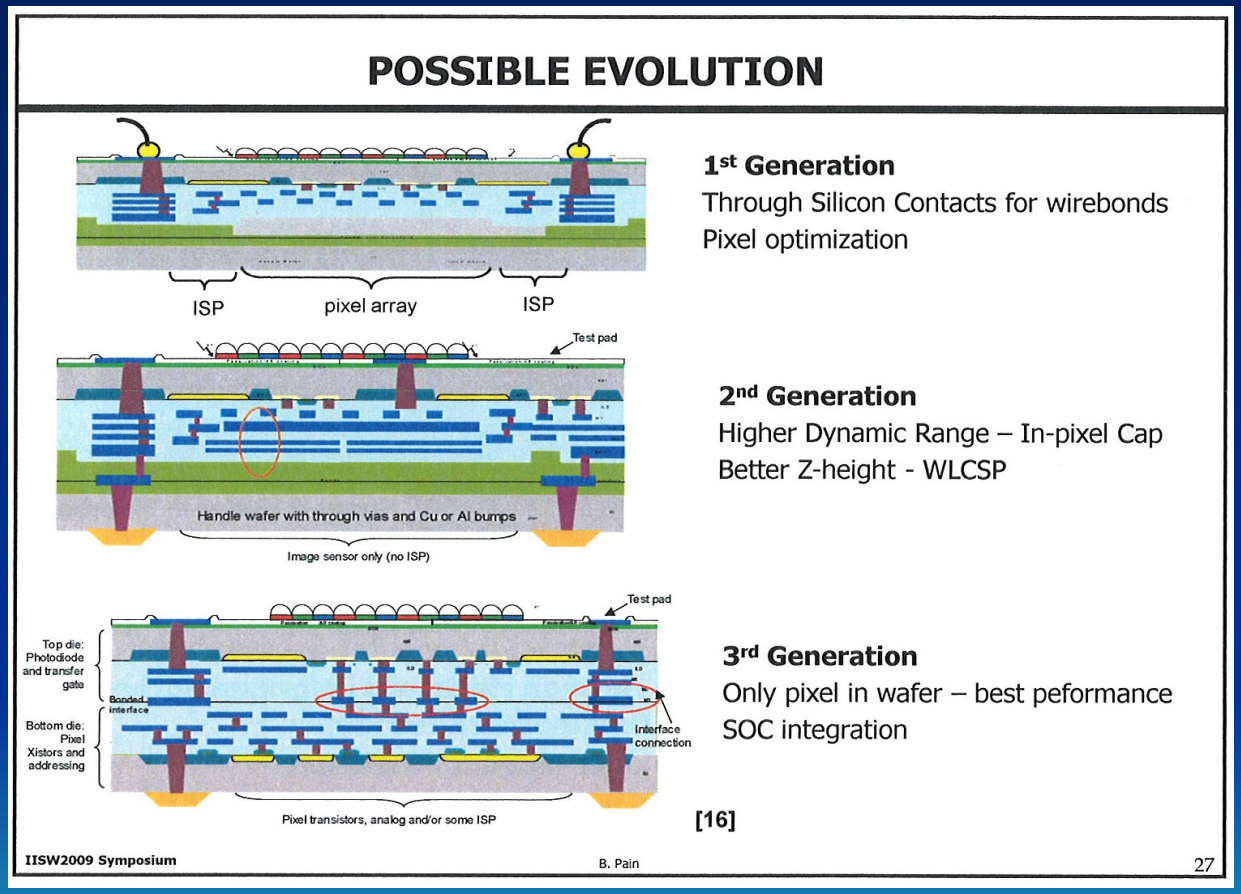
Disadvantages:

- Cost and availability of SOI wafer material
- They have not yet managed to produce high volume reliably

Commercial Thinning (3)



3 D stacking (R&D / commercial) MIT / IMEC ST, TSMC….



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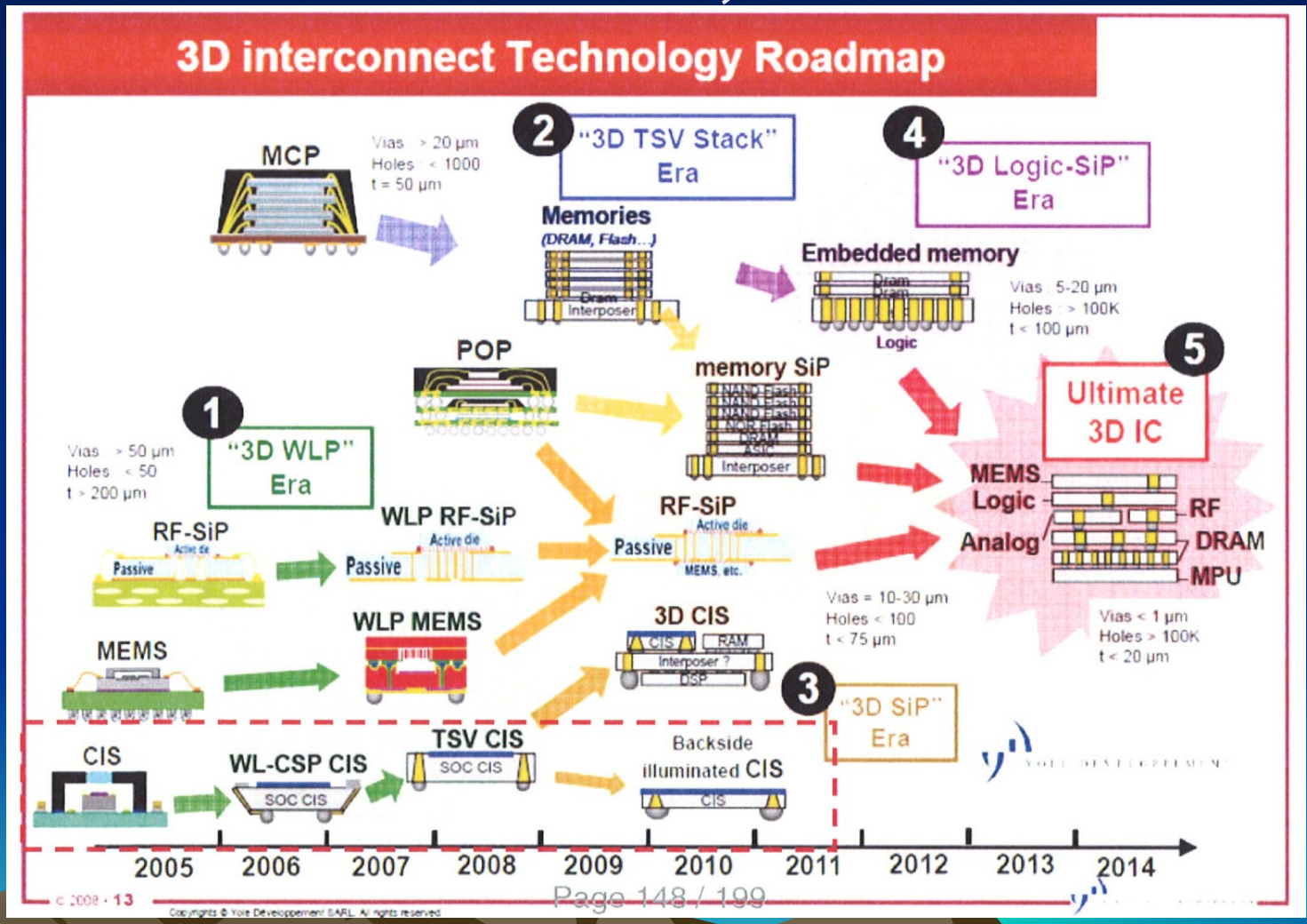

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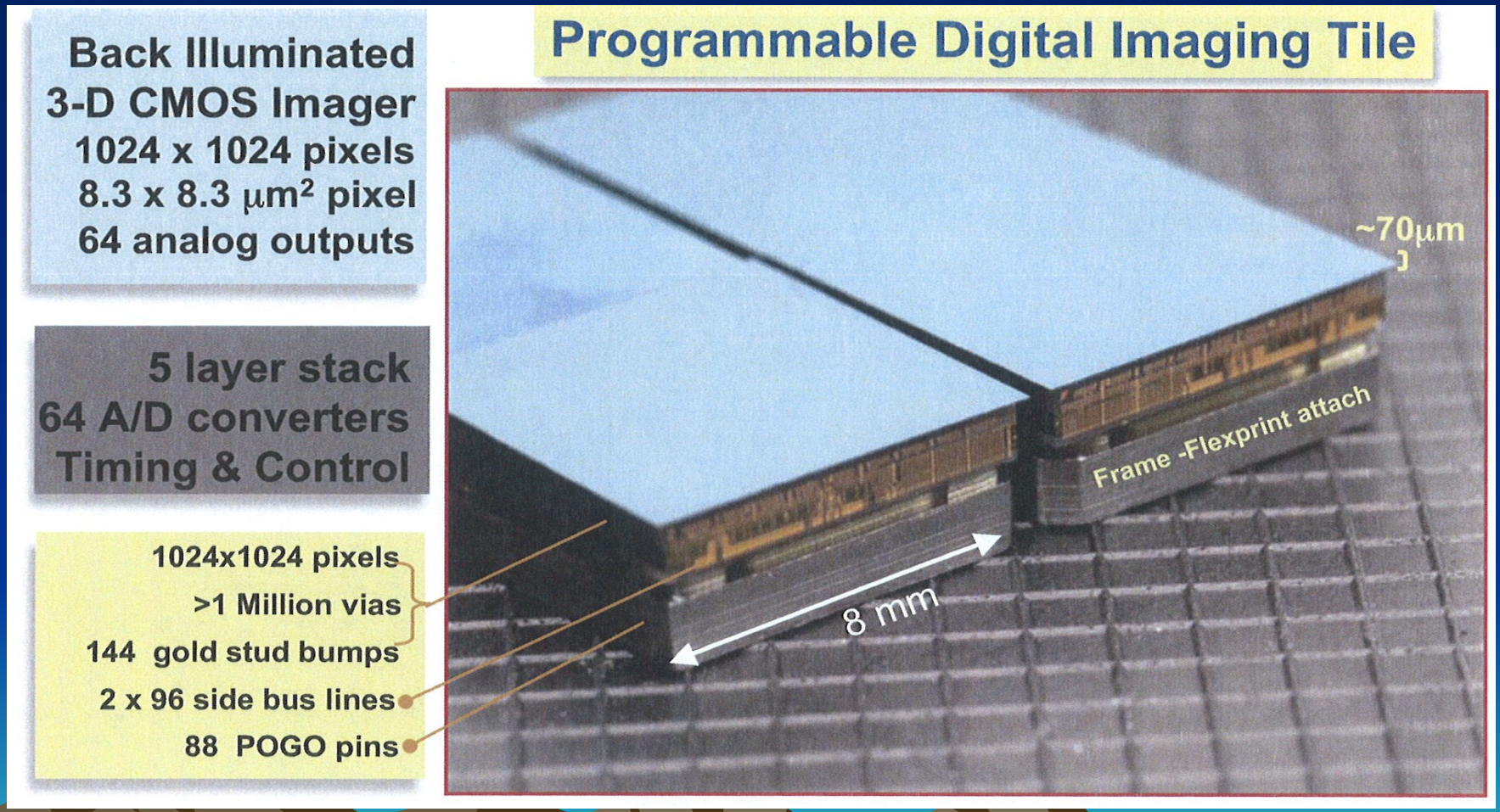
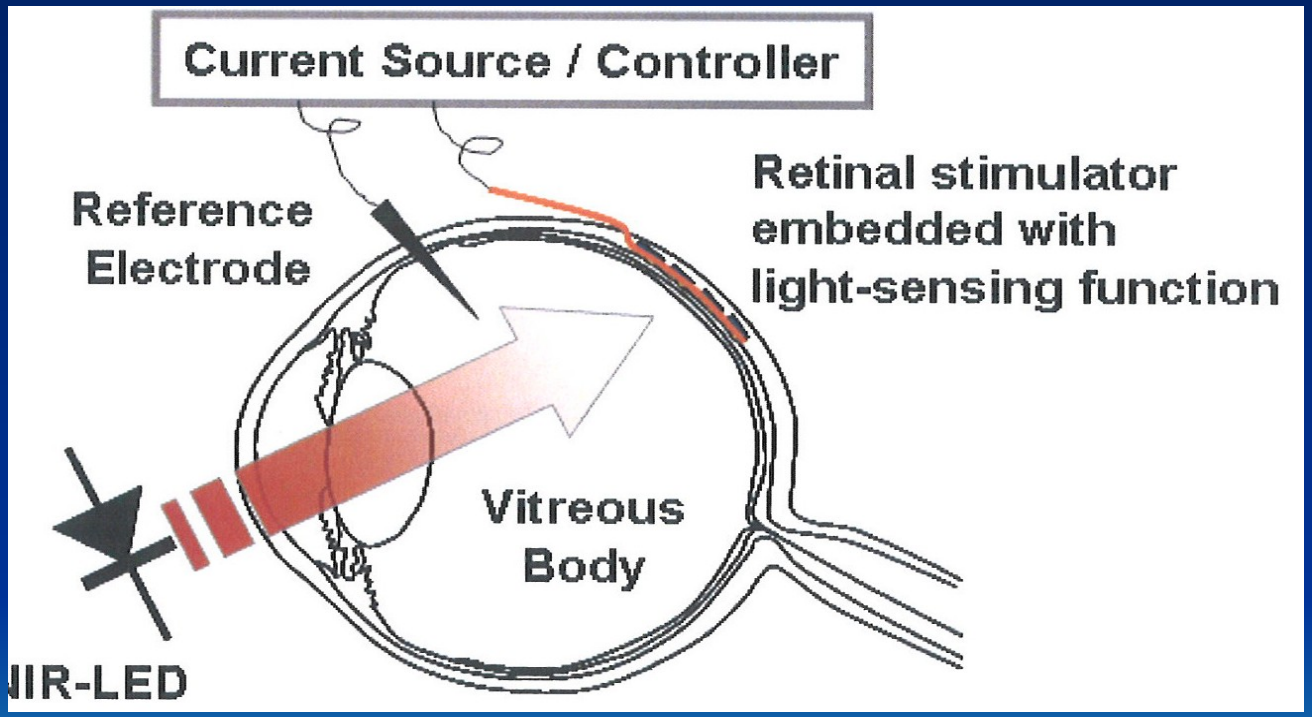


Other CMOS applications (1) Medical market

- Large CMOS 3x2 mosaic xray panels:
  23x29 cm, RON typically 175e-, pixelpitch 25-70 um, 5-10 frames/s, DQE 10%
- Tiny CMOS: Video endoscopy
- alternatively ‘pill camera’ (but not positionable)
- Artificial Seeing: Retina stimulator with CMOS detector

Other CMOS applications (1) Medical market

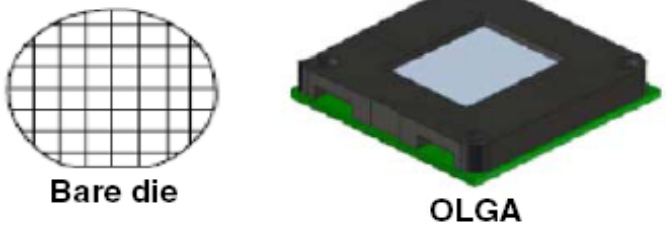
Other CMOS applications (1) Medical market



Other CCD/CMOS applications (2)

- High speed video capture with CCD buffer and CMOS readout (problem small storage time)
- U-HDTV sensors (Mark)
- CMOS no rolling shutter / high speed:
  - Railroad inspection (200 - 250 km/h)
  - Crash Test high speed camera (precise optical measurement)
- (Photo finish camera (also CCD L3 technology)
- CMOS Rolling shutter:
  - General Automotive
  - Inspection devices for
  - semiconductor / LCD panels,
  - rubber sealis etc.
  - fingerprint sensors

Other CCD/CMOS applications (2)



Applications

- Adaptive cruise control/stop and go
- Pedestrian detection and protection
- Headway/forward collision warning
- Pre-crash active safety
- Lane departure warning
- Lane keeping
- Night vision (NIR - Near InfraRed)
- Automatic high/low beam control
- Lane change assist
- Blind spot detection

New commercial trends

Computational photography / light field camera:

- Microlens & oversampling detector, which reconstructs the ray pattern and recalculates unfocussed areas into focussed ones after the exposure
- Please look at: www.refocus-imaging.com

Electro-optical ray tracing with www.lumerical.com superior to CodeV ?

Even in commercial low cost ‘toy’ products there are advantages seen for conventional shuttering and autofocus (opposed to rolling shutter and fixed focus now)

- More commercialization of autofocus and shutter by means of fully integrated MEMS devices: Please look at: www.siimpel.com
- Micro-Electro-Mechanical Systems (MEMS) is the integration of mechanical elements, sensors, actuators, and electronics on a common silicon substrate through microfabrication technology. The micromechanical components are fabricated using compatible "micromachining" processes that selectively etch away parts of the silicon wafer or add new structural layers to form the mechanical and electromechanical devices.

New commercial trends