An Overview of AONGC and the ESO Adaptive Optics Wave Front Sensing Camera

Javier Reyes[a], Mark Downing[a], Ralf Conzelmann[a], Leander Mehrgan[a], Joerg Stegmeier[a], Mirko Todorovic[a], Ignacio Molina-Conde[b]

[a]ESO - European Organisation for Astronomical Research in the Southern Hemisphere, Karl-Schwarzschild-Str 2, 85748 – Garching near Munich, Germany ; [b]Electronic Technology Dept., University of Malaga, Campus de Teatinos, 29071 - Malaga, Spain

ABSTRACT

The detector controller requirements for Adaptive Optics (AO) cameras presents numerous challenges in the design of the electronics, all of which have led to highly customized controller development in order to meet the requirements of high frame rate, low-noise and low image latency in a compact sized camera.

This paper presents an overview of the ESO AOWFS camera and AONGC, the Adaptive Optics ESO's new detector controller; the challenges and excellent progress in achieving detector limited performance from the e2v EMCCD CCD220, along with test results demonstrating sub-electron read noise at frame rates in excess of 1500 Hz. Pre-series cameras have been delivered for use in 2nd Generation VLT instruments (AOF and SPHERE).

Keywords: e2v, L3Vision, CCD220, EMCCD, Adaptive Optics, Wave Front Sensing, High-voltage clock, AONGC

1. INTRODUCTION

Although the ESO AOWFS camera focuses on only one type of detector the challenges in the design of the camera are various. In addition to the challenges related with driving an L3Vision CCD such as the generation of up to 50V high-voltage sine wave clock for the multiplication register and high-speed clock drivers for the serial phases, its compact size of only 235 x 190 x 75 mm imposes tight constraints on the electronics integrated inside, the electronics board arrangement and the total heat dissipation. Moreover, the high read-out speed adds an extra challenge to the sequencer which must run at sub-nanosecond timing resolution (78ps) which imposes that the digital electronics must be in close proximity of the detector.

In addition, the AONGC electronics must interface via dedicated fiber links to two different (wavelength, rate and protocol) nodes, namely the control LLCU (Linux PC that takes care of the camera control, telemetry and configuration) and to the ESO SPARTA[5] real time computer.

The camera is a self-contained line replaceable unit (LRU) with extensive housekeeping capabilities like moisture, pressure, and temperature sensors on CCD package, water cooling block and electronics.

2. SYSTEM ARCHITECTURE

2.1 System Architecture

See Figure 1 for an overview of a single-head camera system. On the front-end side, the components comprising the minimum detector system are the WFS camera head (1), the power supply (2) and the Peltier controller (3). On the back-end side the components are a 19-inch control PC running Scientific Linux (4) and a 64-bit/33MHz PCI-Express board (5). The LLCU takes care of commanding the camera via single-mode optical fiber (7) whereas the CCD raw frames are sent for processing via a multi-mode fiber (8) to the ESO real-time number cruncher SPARTA (6).

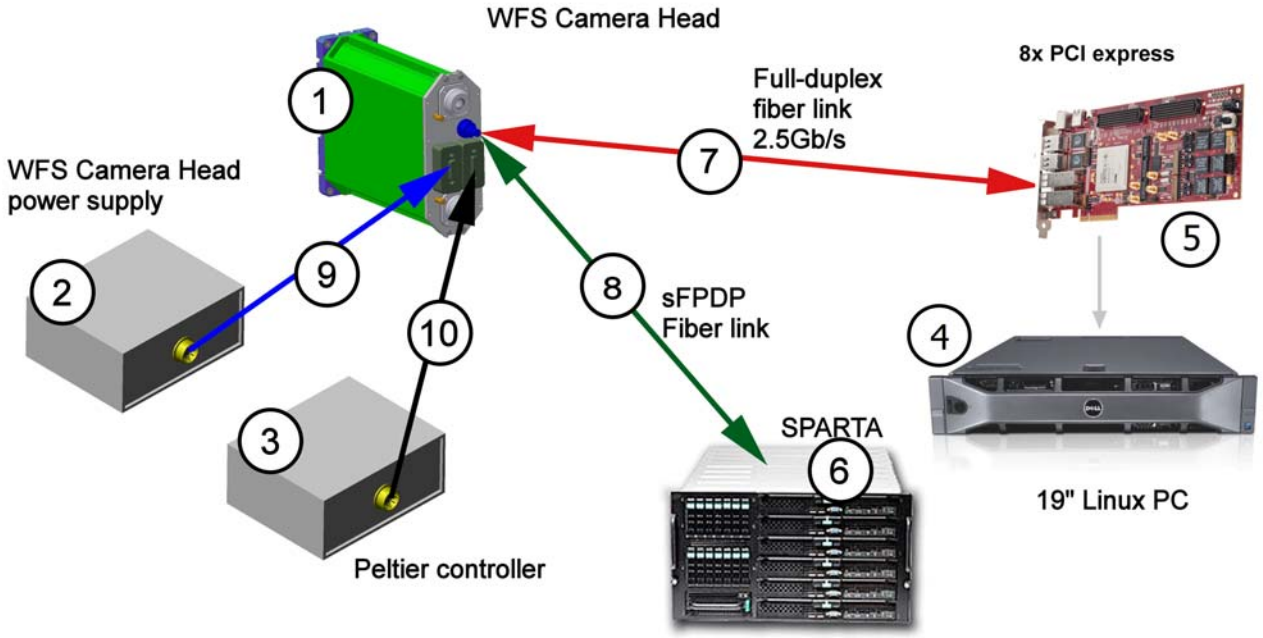

Figure 1: System architecture overview.

2.2 Multi-head connection architecture

The camera can operate both in stand-alone mode as shown Figure 1 (e.g. tip-tilt) or synchronous with other heads in a multi-head scenario. In a multi-head configuration, the cameras are connected in daisy chain configuration and controlled by a single LLCU either with a single PCI-e interface card, or several cards. Independently of the configuration each head runs its own sequencer and transmits the raw image frames simultaneously and independently to SPARTA. The cameras can run synchronously or asynchronously.

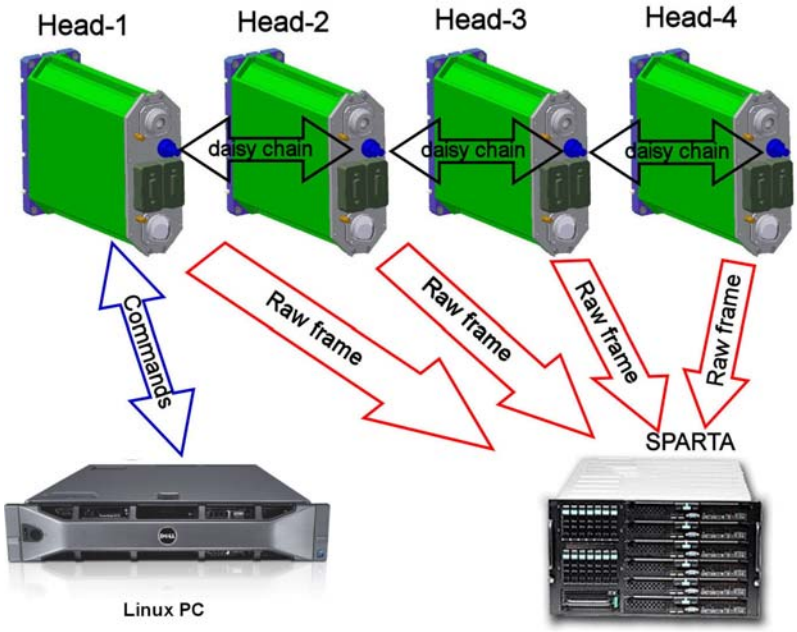

Figure 2: Multi-head connection architecture.

3. AOWFS CAMERA HEAD ASSEMBLY

Figure 3 and Figure 4 shows the interior of the camera head.

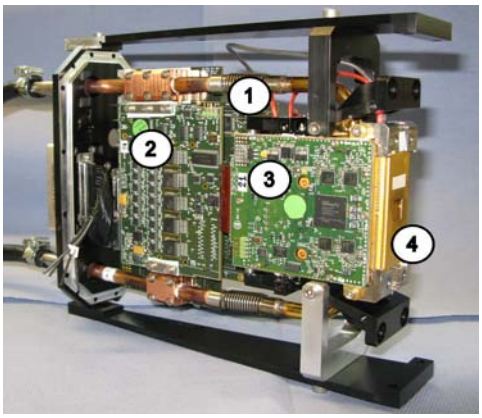

Figure 3: AOWFS camera showing ***1)*** Main board, ***2)*** Bias board, ***3)*** AD board left, ***4)*** CCD220.

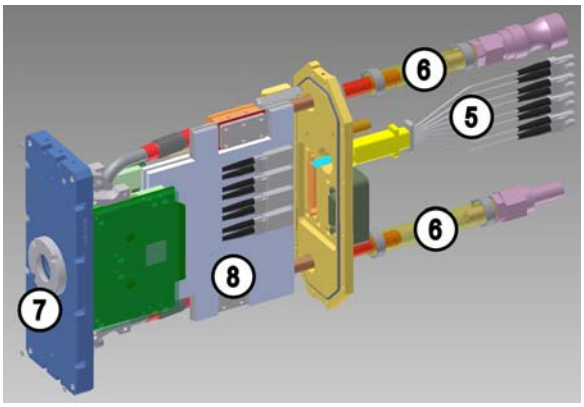

Figure 4: AOWFS camera showing ***5)*** Fiber feed-through, ***6)*** Water cooling pipes, ***7)*** CCD window, ***8)*** Rear side of Main board.

4. AOWFS ELECTRONICS

The AOWFS electronics is an assembly of 6 boards, 5 out of which are different. The boards are called: AONGC main board, Bias board, AD board (two identical boards per camera), Clock driver board left and Clock driver board right. The description of these is explained below.

AONGC main board: This is the main board and the heart of the electronics. It serves as the data and command interface to the LLCU and SPARTA. It contains the sequencer. In addition, it takes care of housekeeping functions like humidity, temperature, pressure sensing and temperature alarms, to mention a few. In addition to all this on this board, the three-level clocking takes place for the image and storage CCD areas. The front and back side of the board can be seen in Figure 5 and Figure 6.

Figure 5: AONGC Main board top. The big thermal pads connect the PCB to the thermal cooling pipes via copper clamps.

Figure 6: AONGC Main board bottom. On the upper side of the board one can see the low-profile optical transceivers LNP-LT12HB (1320nm) and LNP2-ST11HB (850nm), see reference [6].

Bias board: Due to volume constrains the Bias board is piggy-backed on top of the Main board. The purpose of this board is to generate the bias voltages to bias the CCD220 (VRD, VOD, RØDC, VOG) and the DC upper and lower rails of the clocks that drive the CCD (ØR, ØC, RØ1, RØ2, RØ3); see reference [7] for the details. These upper and lower rails are switched on the Clock driver boards. There are three types of DC voltages generated on the Bias board. 1) Normal DC bias voltages with low current demand by the CCD, 2) Medium current DC bias voltages (VØR, VØC) and, 3) High-current DC bias voltages for the VOD, CCD reset gate (ØR), and the voltages levels (SDL and SDH) of clocks that control the shutter of the shuttered version of the CCD220, the CCD219. This board is shown in Figure 7 and Figure 8.

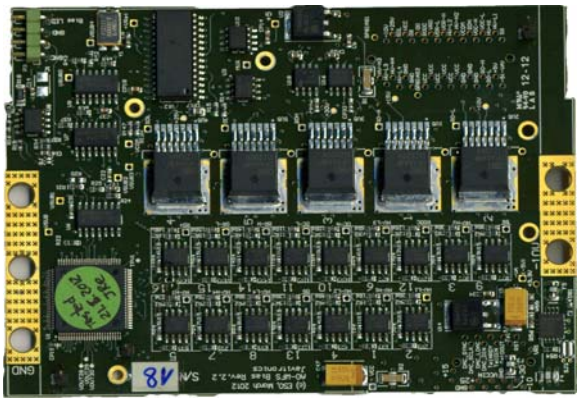

Figure 7: Bias board top. As on the Main board the left and right thermal pads are connected to the cooling pipes.

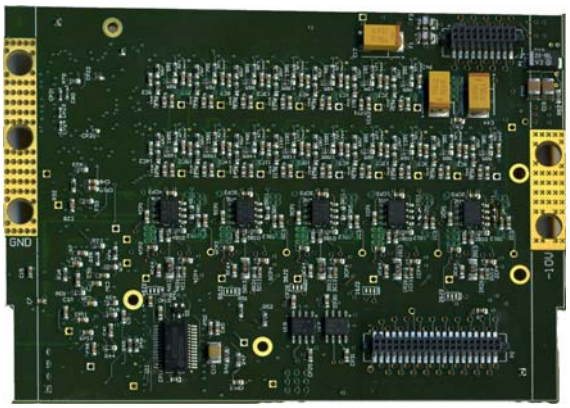

Figure 8: Bias board bottom.

AD board: This board contains the CCD output signal amplifier, the analog front-end ADCs, and a low power FPGA (Spartan-6 XC6SLX25). The input amplifier gain is around 4.8 that with a CCD output amplifier responsivity of 1µV/e- gives a video signal at the input of the ADC of about 4.8µV/e-. The analog front-end ADCs are based on a 14-Bit 30 MSPS CCD Signal Processor (AD9824) containing an input clamp and a correlated double sampler. The task of the FPGA is many fold, it takes care of the control of the ADCs, the serialization of the pixel data stream going to the Main board, and, the over-illumination protection (see section 4.2). Figure 9 and Figure 10 show this board.

Figure 9: AD board top. The board is connected to the Main board via a flex PCB.

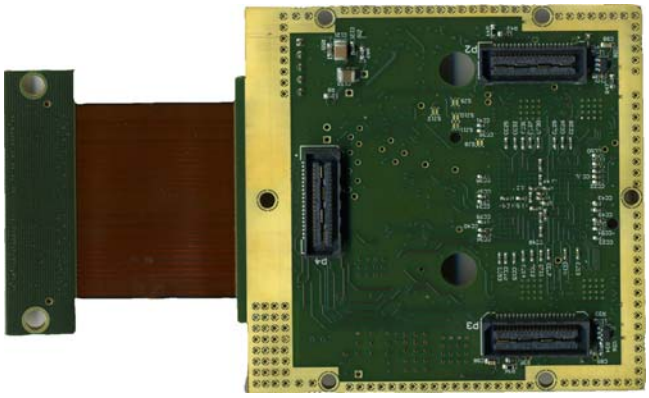

Figure 10: AD board bottom. The three connectors on the bottom side interface with the clock driver board.

Clock driver board left: This board contains two high-voltage resonant circuits for the CCD220 multiplication registers (RØ2HV1, RØ2HV2), the high-speed drivers for the output amplifier clamp (ØC), the reset clock (ØR) of the CCD, and the driver for the parallel phases of the CCD image (IØ1, IØ2) and store (SØ1 and SØ2) regions.

Figure 11: Clock board top. The three connectors interface this board to the AD board.

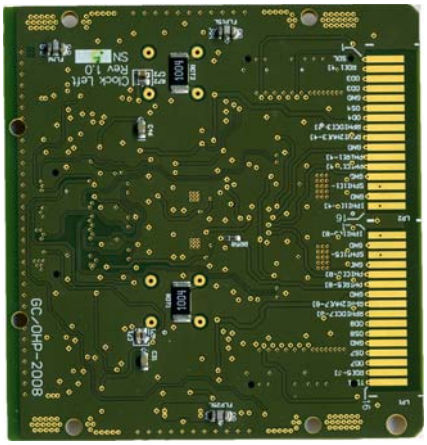

Figure 12: Clock board bottom. On the left side one can see the pads for the spring contacts that connect to the CCD.

Clock driver board right: Similar to the Clock driver board left, this board contains the other two high-voltage resonant circuits for the CCD220 multiplication registers (RØ2HV3, RØ2HV4), the high-speed drivers for the serial phases (RØ1, RØ2 and RØ3) and the drivers for the parallel phases of image (IØ1, IØ2) and store (SØ1 and SØ2). These are the same signals but inverted as on the left side of the CCD. Figure 11 and Figure 12 show the two sides of Clock driver board. In the right side of Figure 12 one can see where the spring contacts are soldered on the PCB.

It is important to note that both the AD and Clock board are assembled together in what is called the analog front-end. This assembly is shown in Figure 13. The AD and Clock board assembly have a solid copper metal frame which is connected to some hot components on the Clock board and to the cooling block where the CCD is sitting.

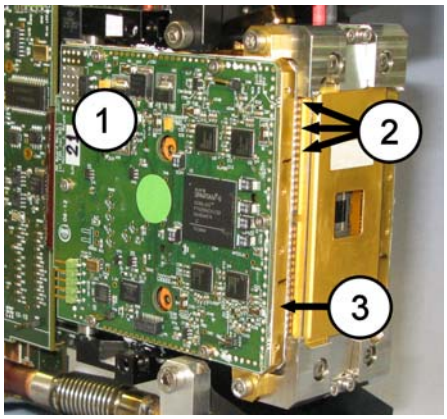

Figure 13: AD board and Clock driver assembly. ***1)*** AD board, ***2)*** Contacts on the Clock board, ***3)*** Copper frame thermally connected to the cooling block.

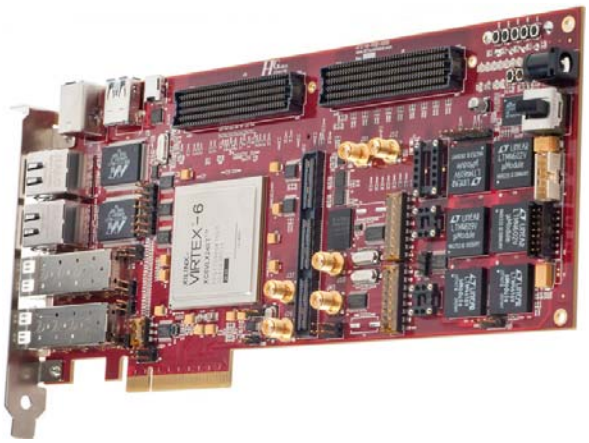

Figure 14: COTS PCI-e board on the back-end PC Linux computer.

PCI Express board: This board belongs to the back-end computer. It is a Commercial-Off-The-Shelf (COTS) from HighTech Global[9] featuring among other things a Virtex-6 XC6VLX240T, two Small Form-Factor Pluggable (SFP) fiber modules, two 10/100/1000 Ethernet ports, a bank of DDR3 SODIMM memory, SubMiniature version A (SMA) RF connectors, and a FPGA Mezzanine Card (FMC) interface for user application hardware.

4.1 Reshape of the AONGC front-end boards

In order to simplify the electronics design and improve its manufacturability, reliability, maintenance and thermal performance, the AD and Clock board described above are currently being combined into one single board called the AFE board. This board reshaping has been done in collaboration with FLI (First Light Imaging), see reference [8].

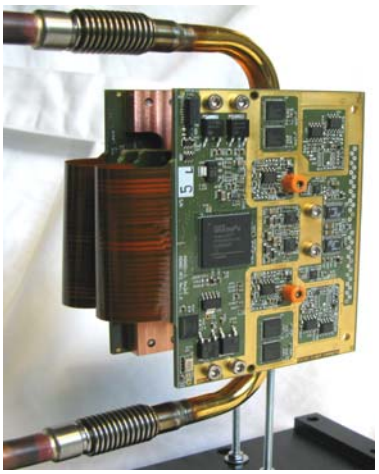

Figure 15: Front-end reshaped board combining the old AD and Clock boards.

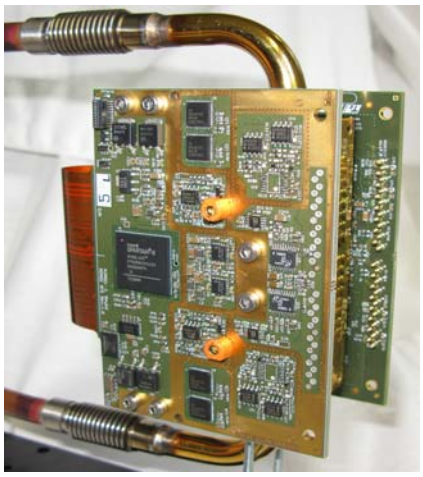

Figure 16: Another view of the front-end reshaped board.

4.2 Camera mechanics

The mechanical joint of the parts are sealed air tight and the camera is flooded with nitrogen at about 1.5atm in order to avoid the ingress of moisture inside the camera resulting in water condensation. The electronics features small sized humidity, temperature and pressure sensors to monitor the internal camera environment and to provide alarms in case of overtemperature, high humidity or loss of pressure.

4.3 CCD protection from over-illumination

The CCD220 is an EMCCD (Electron Multiplication CCD) with gain in the serial register by impact ionization which can result in aging or damage due to over-illumination. The camera features two ways of preventing the over-illumination to happen. At high-speed and in real time, the AONGC firmware on the AD board inspects each pixel value in the data stream to detect saturation. If the number of saturated pixels exceeds a limit, e.g. 300, per port and per frame, the electronics turns down the gain to avoid the damage or premature aging of the CCD. In addition and at much lower speed, AONGC electronics senses the global (IRD) current flowing from the CCD to detect over-illuminated frames, and again turns down the gain to avoid problems..

4.4 Camera thermal protection

In addition to the voltage supervisor described in the power supply description, section 5.1, the power supply contains a passive thermal protection circuit based on a bimetal that will shutdown the whole power supply unit if the temperature on the cooling block (where the CCD is mounted) goes above 40°C. If the thermal protection triggers, the power supply must be rearmed manually, however, the power supply will not go on-line until the temperature on the CCD cooling block goes below the trip point.

In addition, the camera is equipped with an active circuit which will avoid powering up the electronics if the temperature on the cooling block is above 40°C (configurable by firmware) or below -8°C (the water cooling is nominally 8°C below ambient temperature). The upper limit of the temperature can be due to lack of water coolant or some other problem inside the camera whereas the lower limit of the temperature may be an indication of some other anomaly inside the head, e.g. temperature sensor broken or detached from the cooling block. The camera thermal protection runs autonomously and does not depend on any other circuit inside the camera, the firmware or the proper functioning of the

FPGA. This thermal protection is based on a 16-bit low power consumption mixed signal microcontroller (MSP430F2013, see reference [4]) connected to a current output temperature sensor, Analog Devices AD590, glued on the back of the cooling block. The microcontroller senses the temperature and controls an opto-coupler which triggers a relay inside the power supply unit. A thermal error condition inside the AOWFS head, triggers as error condition in the power supply voltage supervisor that leads to the shutdown of the camera power supply.

4.5 Camera Environmental Sensors

In order to avoid condensation, the camera is equipped with a SHT15 fully calibrated relative humidity (12-bit resolution, ± 2.0%RH accuracy) and temperature (14-bit resolution, ± 0.3%) sensor from Sensirion, see reference [1] for details. This dual sensor is read continuously by the firmware on the Main board and the humidity and temperature are stored in registers that is monitored by the upper level software running on the LLCU. In case that the humidity or temperature are out of software predefined limits, an alarm will be issued and the operation of the camera will be stopped.

The camera also contains a solid-state absolute pressure sensor from Freescale, see reference [2]. The pressure sensor selected is the MPL115A2 with a range of 50 to 115 kPa. Similarly to the humidity/temperature sensor, this sensor is continuously read by the firmware and its reading is stored in a register monitored every second by the control software on the LLCU. The camera is pressurized with nitrogen and in case of loss of pressure, the control software will issue an alarm and the operation of the camera will be stopped. Figure 17 shows the GUI displaying the camera working conditions.

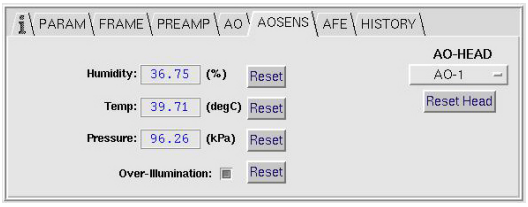

Figure 17: Environmental sensors panel. This panel also contains the over-illumination indicator.

5. POWER SUPPLY AND PELTIER CONTROLLER

5.1 Power Supply

The power supply unit contains 7 individual linear power supplies from Kniel (2V digital, 3.6V digital, and -10V, 3.6V, 15V, 25V and 30V analog) mounted in a 19" rack. Each power supply rack contains 2 separate power supply units and therefore is able to power up two independent camera heads. The front and back of the power supply is shown in Figure 18 and Figure 19.

Figure 18: Front side of the power supply showing the two MIL circular output connectors on the left side.

Figure 19: Rear side of the power supply showing the voltage supervisors on either side, one for the front set of power supplies ***1)***, and the other for the rear ***2)***.

The power supply rack is equipped with a voltage supervisor to guarantee that all power supply voltages are within the permitted voltage range. Any voltage going out of the allowed limits, including a short circuit, will shutdown the

complete power supply unit. In case of failure of any of the power supplies the power supply unit can be rearmed by power cycling the unit or by pressing the reset button on the front-panel of the voltage supervisor.

5.2 Peltier controller

The Peltier controller is built around the process and program controller JUMO IMAGO 500, see reference [3] for details. The AOWFS Peltier controller is able to control two camera heads independently. It runs autonomously and has a single switch on the front panel to warm up and cool down the CCD according to a predefined profile. Although the temperature set point is adjustable, the unit is nominally configured to cool down the CCD to -40°C. The user simply flicks the switch to the "cool" position to cool down the CCD, or conversely, to the "warm" position to warm up the CCD. The cool/warm process takes about 5 min (defined by a fully programmable software profile). The display of the unit shows the temperature of the CCD and the cooling block (basically the temperature of the water coolant), the temperature set point and the current being delivered to Peltier. The current to the Peltier is provided by a 8V, 4A linear programmable (by the Peltier Controller) power supplies from Kniel.

Figure 20: Front panel of the Peltier controller. ***1)*** Output for the first camera head. ***2)*** Alarm output and external input connectors. ***3)*** JUMO Imago 500 controller. ***4)*** Output for the second camera head. ***5)*** Serial communication and maintenance connectors.

Figure 21: Peltier controller display screen.

6. AONGC SOFTWARE

Although the electronics of AONGC and ScNGC (ESO controller for scientific applications) are completely different and share no commonality, the software of both is almost identical. That means that at the user level both systems are operated in a very similar way.

Figure 22 shows the GUI panel to configure, control and monitor the camera head. From this panel the CCD voltages can be adjusted for optimization purposes, the CCD phases can be shifted (see Figure 24 and Figure 25) and the environmental sensors can be monitored (see Figure 17). As part of the software to support the programming of any CCD sequencer, a self-contained graphical interface called Bluewave has been developed, see Figure 23.

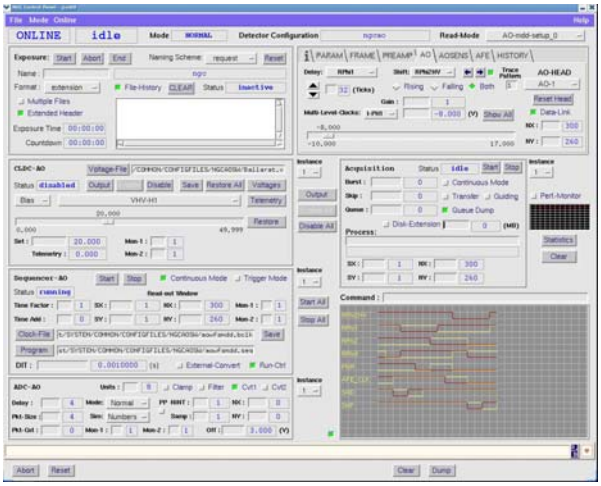

Figure 22: Camera control software.

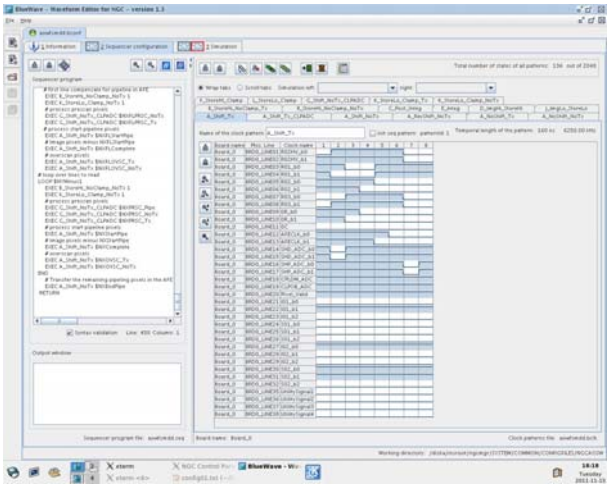

Figure 23: Bluewave, a sequencer and clock pattern programming software.

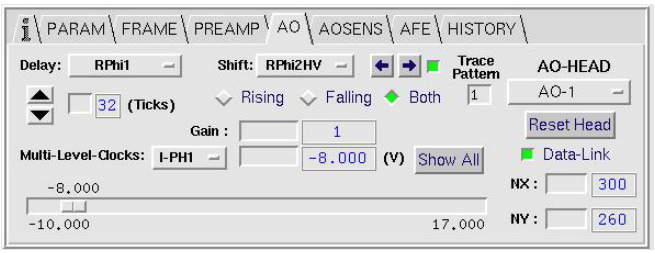

Figure 24: AONGC phase and clock delay panel.

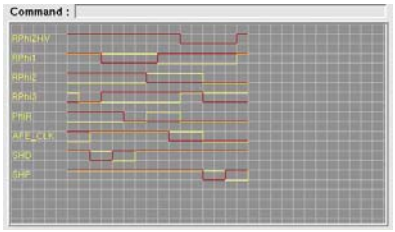

Figure 25: CCD phase programmed and actual phase on the CCD chip after taking into account the delay.

7. A GLIMPSE OF AO SYSTEMS USING THE AOWFS CAMERA

Figure 26 shows a typical lenslet pattern of the camera in operation.

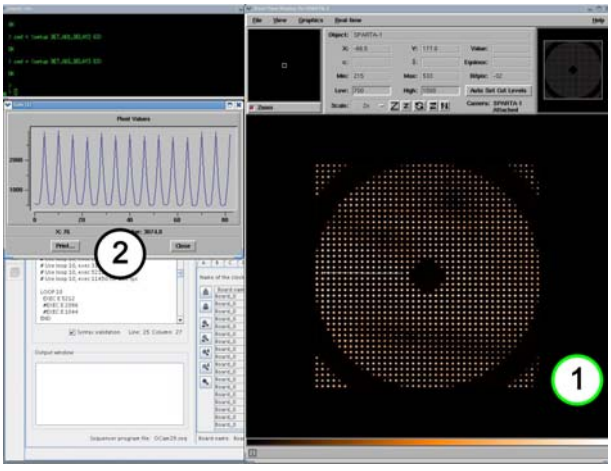

Figure 26: Typical AO image on the RTD (Real Time Display).

Figure 27 shows the four AO cameras mounted on GRAAL. GRAAL is based on a four Sodium Laser Guide Stars (Na-LGS) system launched from the corners of the centre piece of a Unit Telescope of the VLT. The AO-loop is closed at a 700 to 1000 Hz frequency.
Figure 28 shows GALACSI. It is mounted to the same four Sodium Laser Guide Star system. Its AO-loop is closed at frequency of 1000 Hz.

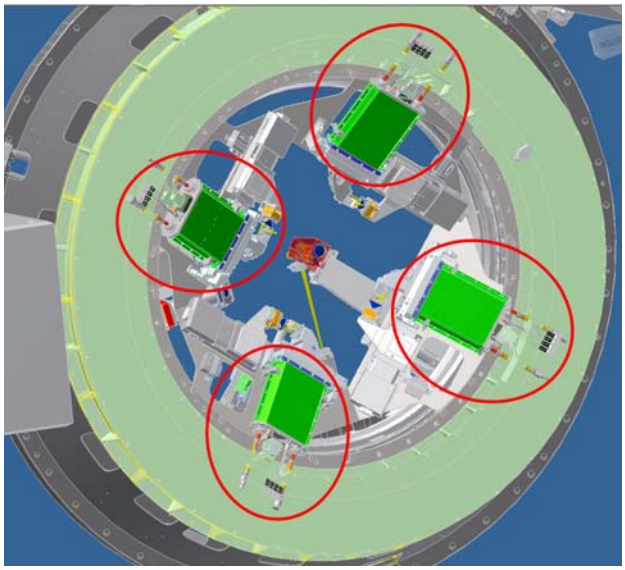

Figure 27: ESO AOWFS cameras on GRAAL. Two additional ones (Tip/tilt and MCM camera) are not visible.

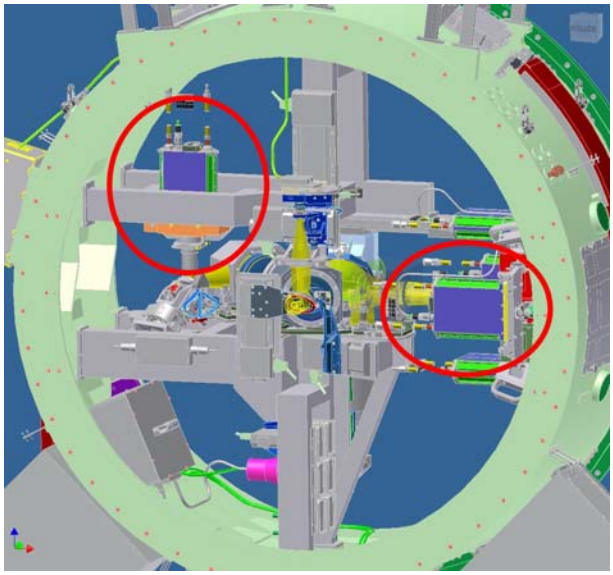

Figure 28: GALACSI with two of the four AO cameras highlighted. (Tip/tilt camera not visible)

8. ESO AOWFS CAMERA SUMMARY

CCD Technology	e2v L3 Vision
Format	240 x 240, 8 output ports
Pixel size	24 x 24 μm^2
RON (high gain mode)	< 0.1e- (0.2 goal)
Frame rate	1.5kfps (1.2kfps nominal)
CCD temperature	<-40 °C
Video chain ADC	14-bit
Digital electronics	Xilinx Virtex-5 @ 200MHz
Sequencer	200MHz, 5ns ticks, 78ps resolution
Link to PC	1310nm fiber link at 2.5Gb/s. Xilinx Aurora protocol
Link to SPARTA	850nm fiber link at 3.125Gb/s 1.4 Gb/s pixel rate sFPDP protocol (V-Metro)
Camera head size	235 x 190 x 75 mm
Camera head weight	3.5kg approx
Gas filling	Nitrogen, flushed with a pressure difference of ~ 0,5bar

REFERENCES

[1] http://www.sensirion.com/en/products/humidity-temperature/humidity-sensor-sht15/.

[2] http://www.freescale.com.

[3] http://www.jumo.de/

[4] http://www.ti.com/lsds/ti/microcontroller/16-bit_msp430/overview.page

[5] "SPARTA for the VLT: status and plans", Suárez, M., Fedrigo, E., SPIE Proc. 8447-98, (2012)

[6] http://www.stratos.com/

[7] http://www.e2v.com/products-and-services/high-performance-imaging-solutions/imaging-solutions-cmos-ccd-emccd/

[8] http://www.firstlight.fr/

[9] http://www.hitechglobal.com/