ESO Adaptive Optics Prototype Controller for the E-ELT

Javier Reyes[1], Mark Downing[1], Jorge Romero[2]

[1]European Organization for Astronomical Research in the Southern Hemisphere

[2]University of Malaga

www.eso.org

Abstract

This poster presents the currently under development detector controller for the Adaptive Optics imager in the E-ELT which is based on the e2v Natural Guide Star Detector (NGSD) and Laser Guide Star Detector (LGSD). The detector controller requirements present important challenges in the design of the electronics due to the low-power, low-noise and high parallel data rate of the detectors involved. The general architecture of the controller along with the front-end electronics to drive and read-out the detector are described here. This electronics is based on Xilinx Virtex-6 and Virtex-7 FPGAs.
NGSD is a 880x840 pixel CMOS array organized as 44x42 sub-apertures of 20x20 pixel each. NGSD is exactly 1/4 of the LGSD and therefore it is considered a scaled down demonstrator for the LGSD.

Introduction

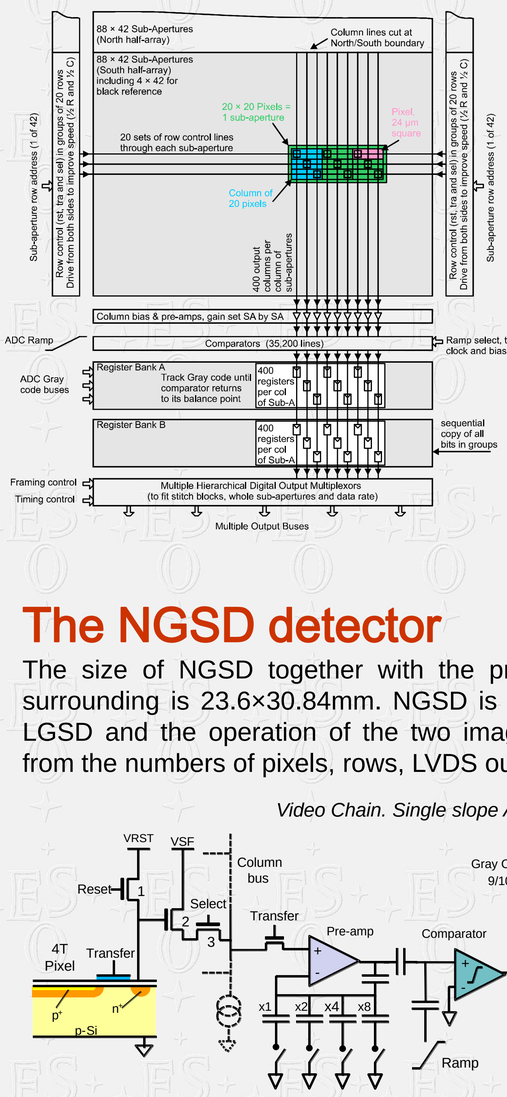
ESO E-ELT Adaptive Optics detectors will be based on a large size new generation 1760x1680 pixels high resistivity CMOS imager sensor called LGSD, Laser Guide Star Detector. Before the development of LGSD, a pioneering quarter size 880x840 pixels Natural Guide Star detector, called NGSD, will be built. Both NGSD and LGSD will have the same pixel architecture and make use of massive parallel Analog-to-Digital structures, as many as 17,600 and 70,400 ADCs for NGSD and LGSD, respectively. In spite of the large size detectors, the frame rate will be above 700fps and the expected read-out noise below 3e-.

NGSD imager is currently in production and ESO expects to receive the first electrical grade front-side illuminated chip at the beginning of next year (2014) and its back-side illuminated version about six months later.

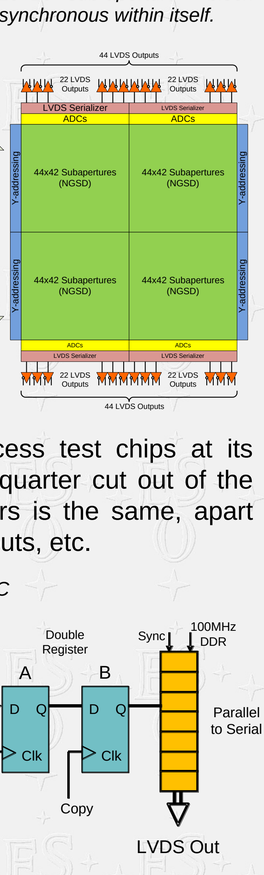
The first prototype controller for NGSD is currently under development and aims at, firstly, the familiarization with the device (both the front- and back-side illuminated imagers) and, secondly, outlining the technology roadmap toward the next generation of ESO controller for AO in the E-ELT environment.

The LGSD detector

The estimated chip size of LGSD is 55x45mm which makes stitching unavoidable. In order to reduce the line rate (1.4ms, 700 fps nominally), the LGSD will be read out as half the array upwards and half downwards which is referred to as the North and South part, respectively. In addition, to further reduce the line rate, the rows in each half will be read out in groups of 20 in parallel, corresponding to stripes of whole 20×20 sub-apertures and giving a snapshot shutter within each stripe of sub-apertures.



These imagers use 20 parallel sets of comparators and registers to read and quantize 20 rows of pixels simultaneously. This feature is needed to achieve the required frame rate and also makes the read of each 20×20 sub-aperture block synchronous within itself.

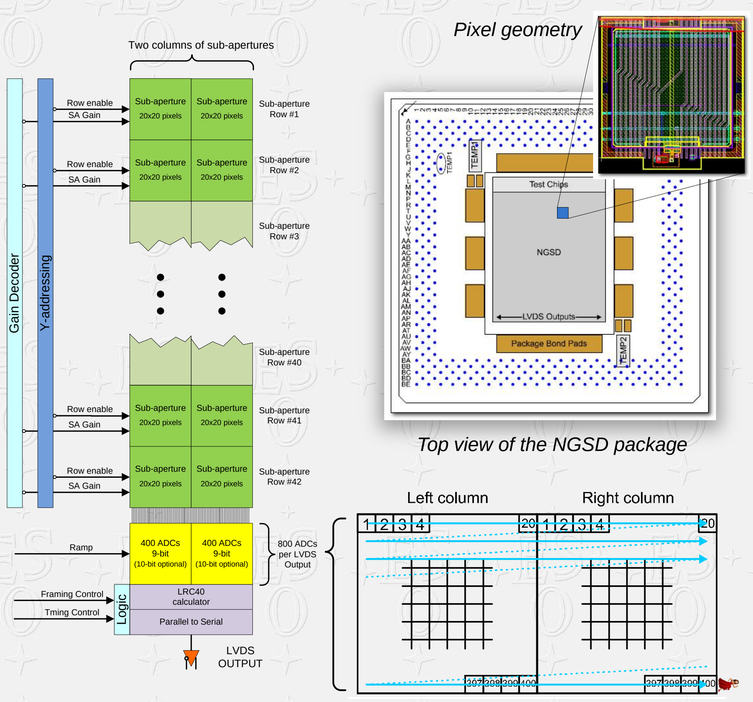


The NGSD detector

The size of NGSD together with the process test chips at its surrounding is 23.6×30.84mm. NGSD is a quarter cut out of the LGSD and the operation of the two imagers is the same, apart from the numbers of pixels, rows, LVDS outputs, etc.

Video Chain. Single slope ADC

Pixel geometry

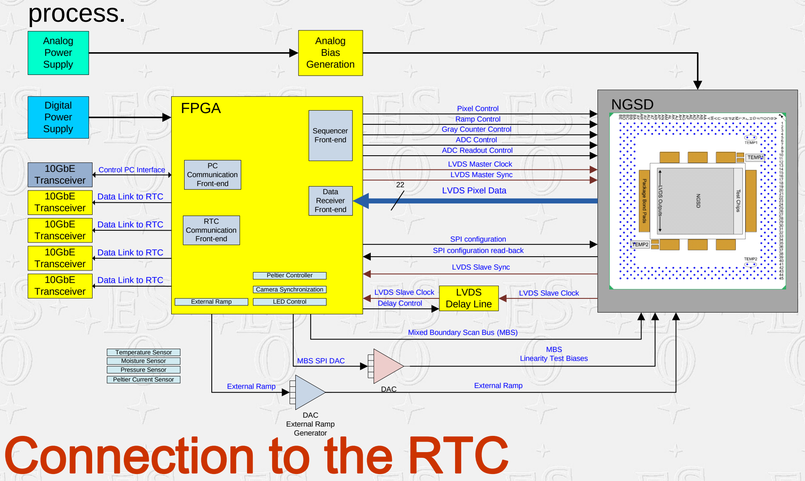


Top view of the NGSD package

Each LVDS output sends the data from two columns of sub-apertures. In order to simplify the wiring on-chip, the bit order from this block of 40×20 ADCs is such that all bit 0 for first row of ADCs are output first, then all bit 1 for the same row and so on until all bits from the row are transmitted before moving on to the next row of ADCs.

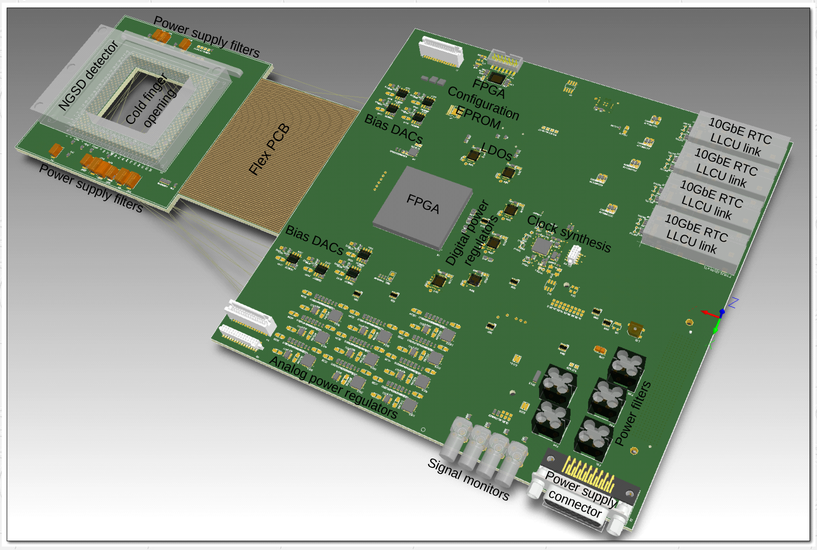
The camera architecture

Since the data conversion and serialization is built-in in the imagers, the camera controller is based on a advanced FPGA with a minimal external analog circuitry (basically, DACs for biasing the detector and its test structures) around it. There is no hardwired sequencer on-chip so almost all critical clocks are individually accessible. Thus, the main tasks of the FPGA are to provide the pixel timing control of the internal ADCs (e.g. pixel reset, preset column, reset preamp, reset comparators and gray code generator) and the timing of the LVDS serializers. As an example of the operation, each time a row of sub-apertures is read, its Y-address must be uploaded over the SPI bus in a data pattern which also includes the gain settings for that row. The SPI runs synchronously to the main data stream readout sequencer process.



Connection to the RTC

The design of the Real-Time-Computer (RTC) for ESO's E-ELT instruments is still under definition and feasibility study but the interface to the controller will be 10GbE using UDP-based protocol or RTSP (Real-Time Streaming Protocol) on top of it in order to allow data broadcasting. The use of 10GbE links for the interface will allow high-performance point-to-point and multicast through Layer 2 commercial off-the-shelf (COTS) network switches which have already been proven to perform deterministically without packet losses. Layer 2 switching is hardware based, mostly based on ASICs, which means that the latency is very low and switching is highly efficient because there is no modification to the data packet, only to the frame encapsulation of the packet. In this context and as part of the forthcoming controller development definition, preliminary tests have already been carried out successfully by Jorge Romero (University of Malaga) to run point-to-point data transmission using UDP and over fiber at 6.25Gbps in a Virtex-6 FPGA using the high-speed GTH serial transceivers.

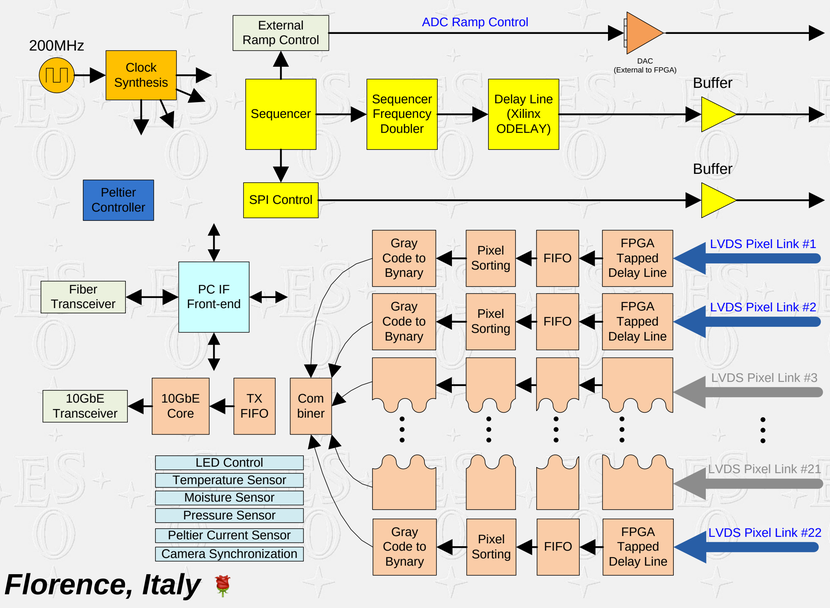


Top view of the NGSD controller under development

The NGSD controller

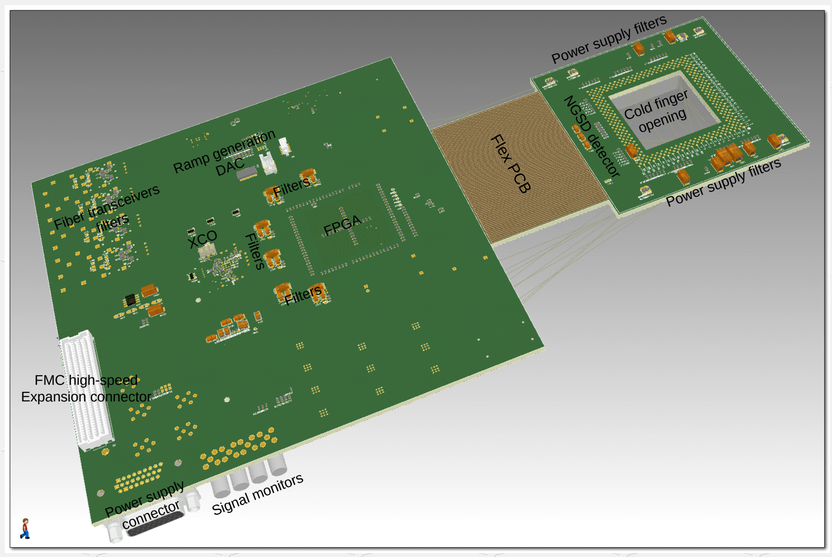
The first version of the demonstration camera for NGSD will be based on the Xilinx Virtex-6 VLX240T FPGA. It is however planned to move to Xilinx Virtex-7 XC7VX690T-2FFG1761C FPGA for both the second version of the NGSD demonstration controller and the controller for LGSD. Among many other features, it is foreseen the provision of circuitry for the synchronization of more than one detector, NGSD and LGSD, to support future multi-camera scenarios in the E-ELT.

Controller Firmware Overview



The LGSD controller

Although the LGSD detector is four times the size of NGSD, the scalability of the controller from NGSD to LGSD presents some additional challenges in its itself, such as electronics power consumption in a small volume, necessity of sub- nanoseconds synchronized read-out between detector halves (not trivial when several high-speed FPGAs are used in conjunction with analog electronics sensitive to noise jitter) and huge data throughput.



Bottom view of the NGSD controller under development

Operation homogeneity

Within ESO, it is key to the operation of a new detector that the user of a new controller experiences no significant difference with its predecessor. In line with ESO's large experience in detector controllers, the NGSD and LGSD demonstration camera will be operated at the user level similarly to AONGC and ScNGC.

Camera mechanics

Similar to the current ESO AO camera based on the CCD220, the NGSD/LGSD camera will be sealed air tight and flooded with nitrogen. The pressure inside will be slightly above the atmospheric pressure in order to avoid the ingress of moisture inside the detector chamber resulting in water condensation. As for the ESO AO camera, this camera will have pressure, humidity and temperature sensors in addition to dedicated over-temperature and over-voltage protection circuitry.

Peltier controller

Both NGSD and LGSD must be cooled at -10degC in operation. The Peltier controller will be part of the demonstration camera and it is planned to have an integrated Peltier controller in order to reduce the number of components and improve the overall dimensions of the camera. It is estimated that 8V and about 3A will be sufficient to cool down the NGSD detector to -10degC with water cooling between 25 and 30degC. From the design of the controller point of view it is still undecided whether the process that controls the current to the TEC will run in an embedded processor inside the FPGA or as a dedicated CPU.

Summary

Item	Value
Detector technology	e2V CMOS
Format NGSD	880 x 840 pixels (44 x 42 SA)
Format NGSD	1760x1680 pixels (88 x 84 SA)
Pixel size	24 x 24 µm^2
RON	< 3e- (<1e- for Ultra Low Vt)
Frame rate	700fps nominal (row time 1.4ms)
On chip ADC	9-bit (10-bit optional), Gray code
Sub-aperture gain	x1, 2, 4 and 8
Pixel Stream Output	NGSD: 22 x LVDS LGSD: 88 x LVDS
LVDS Bit Rate	220Mb/s
Total Throughput	NGSD: 4.752Gbps (2 x 3.125Gbps) LGSD: 19Gbps (4 x 10GbE (TBD))
SPI Configuration	Up to 10Mb/s
FPGA	Virtex-7 XC7VX690T-2FFG1761C (200MHz)
Sequencer	2.5ns ticks, 78ps resolution
Link to PC	1310nm fiber link at 3.125Gb/s. Xilinx Aurora protocol
Link to RTC	UDP 10GbE (NGSD).RTSP goal UDP 4x10GbE (LGSD). RTSP goal.
CCD temperature	-10DegC
Cooling	Peltier
Gas filling	Nitrogen, flushed with a pressure difference of ~ 0,5bar

Scientific Detector Workshop 2013. 7-11 October 2013. Florence, Italy

For more details contact: jreyes@eso.org