FIERA, the new generation of ESO CCD Controllers

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ABSTRACT

This article describes the architecture and the performances of FIERA, the new generation of CCD Controller systems under development at ESO. FIERA is able to run a large number of CCD outputs at fast readout rates, so as to take advantage of the new generation of high speed, low noise CCD readout amplifiers. A FIERA system has been delivered to EEV in Chelmsford, England, for testing the EEV 16 port adaptive optics CCDs, with a burst readout speed of 1 Mps/port (16 Mps total). To our knowledge, this is the first 16 port CCD controller yet made for astronomy.

1) The new generation CCDs.

In recent years the quality of CCD detectors has improved tremendously:

1. CCDs are getting **larger** (2k x 4k are standard CCDs and sizes up to 9k x 9k are being made),
2. new generations of readout amplifiers make it possible to attain **low readout noise** even with fast readout speed (less than 2 electrons noise at 100 kps, i.e. kilopixel/sec, and 4-6 electrons noise at 1000 kps). MIT Lincoln Laboratory and EEV are presently producing the lowest noise amplifiers.

This generates a need for CCD controllers that can read many ports in parallel at high speed:

- the main need for **very low noise** is for *high resolution spectroscopy*,
- **6 electrons of noise @ 1 MHz readout rate** is adequate for *acquisition, focusing, flat-fielding, calibration, direct sky imaging*,
- **fast frame imaging** will allow new kinds of science to be done (e.g., *fast photometry* of rapidly varying objects) and is mandatory for *adaptive optics* systems.

Today it is possible to build electronics that can run any CCD detector or mosaic of detectors that we can envision for the next 10 years.

2) The ESO FIERA CCD Controller

The European Southern Observatory (ESO) must produce about 40 CCD systems in the next few years (see [2]) in order to:

- provide for the instruments of the Very Large Telescope (VLT), a facility of four 8.2 meter telescopes with three 1.8 meter auxiliary telescopes for intereferometry which is under construction on the Cerro Paranal (Chile),
- upgrade the ESO telescopes in La Silla (Chile),
- integrate and test the CCD systems in ESO laboratories.

The most sensible approach for the Optical Detector Team (ODT) at ESO has been to produce a new controller that can optimally operate all the scientific CCDs that ESO acquires for the next 10 years. This controller must be:

1. **universal**, to be able to run all the different CCDs (single or mosaic) in use in ESO's instruments, simplifying system integration and deployment to instruments, and minimizing maintenance;
2. **flexible**, to be prepared for the "next generation" amplifiers that will be only 1-2 electron noise @ 1000 kps readout, and maybe sub-electron noise @ 100 kps;
3. **modular**, to allow expandability, using as much as possible commercially available components.

Our philosophy is that *the performance of the entire detector system should be limited solely to the CCD and the imagination of the user*.

This new advanced controller has been named **FIERA** (**Fast Imager Electronic Readout Assembly**), which means *wild animal* in Spanish, an apt description of this controller, for which no holds were barred as regards speed and flexibility.

3) The FIERA Architecture

The FIERA CCD Controller consists of two modules (see Fig.1 and Fig.2):

1. The **Detector Electronics**, consisting of
    a. A **Communication Board**, for the communications with the rest of the system.
    b. One or two **Analogue Bias Board(s)**.

       Each board produces 16 bias levels that are fully programmable over a range of -15V to +30V. Hardwired protection switches can be used to limit the output voltages which could damage the CCD.
    c. Up to four **Clock Driver Boards** (14 clock lines / board).

       Each board produces up to 14 clocks that can run at rates up to 50 MHz.

       A Clock Driver Board is a mini-motherboard with replaceable modules inserted to produce the clock voltages. Two types of these modules are foreseen to be used with FIERA, to output voltages over the range -12.8V and +12.8V:
        i. a fully programmable bilevel module that outputs 2 voltage levels, with rise and fall times shaped by RC filters,
        ii. a fully programmable multilevel module that can output 256 voltage levels. This will be used in the future to tailor the clock edges to achieve any rise and fall curve desired.
    d. Up to four **Video Boards** (4 channels / board).

       The Video Board includes amplifiers, correlated double sampling (CDS) and analog-to-digital conversion for 4 channels at rates to 2000 kps, with 16 bits per pixel. For the first implementation of FIERA, the clamp-and-sample approach to CDS has been taken, but the design of a Video Board that implements dual-slope is still possible, if needed (see [1]).

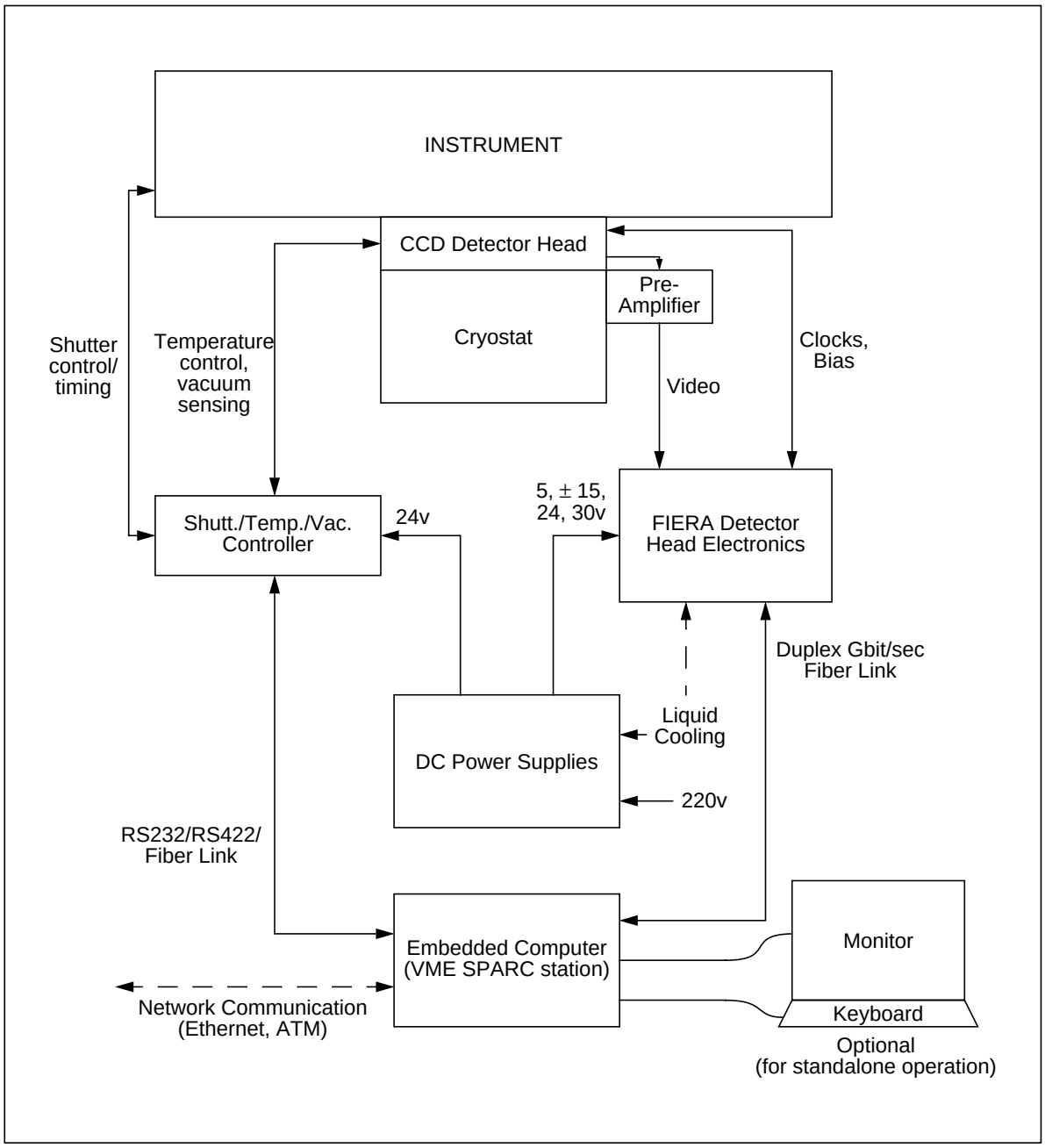

Fig.1 - FIERA system overview

2. The **Embedded Computer**, consisting of
   a. A **SPARC CPU Board**.
   b. A **Detector Electronics Interface Board** (with two DSP TMS320C40), for the communication with the Detector Electronics and real time operations.
   c. An **EDT/SCD20 Data Capture Board**, for fast data acquisition.
   d. A **Local Area Network (LAN) Board**.

   The usage of ATM is foreseen for the beginning of 1998.

e. An (optional) **ESO Time Interface Module (TIM)**.

The TIM provides timing pulses with absolute accuracy of 10 microseconds, as derived from GPS satellite signals.

The Detector Electronics and the Embedded Computer are connected through a 150 MBytes / sec full duplex **optical fiber link** (due to the transmission protocol, the corresponding maximum video data rate is 50 million pixel / sec (Mps), for pixels up to 21 bits wide).

Table 1 summarizes the FIERA System Specifications.

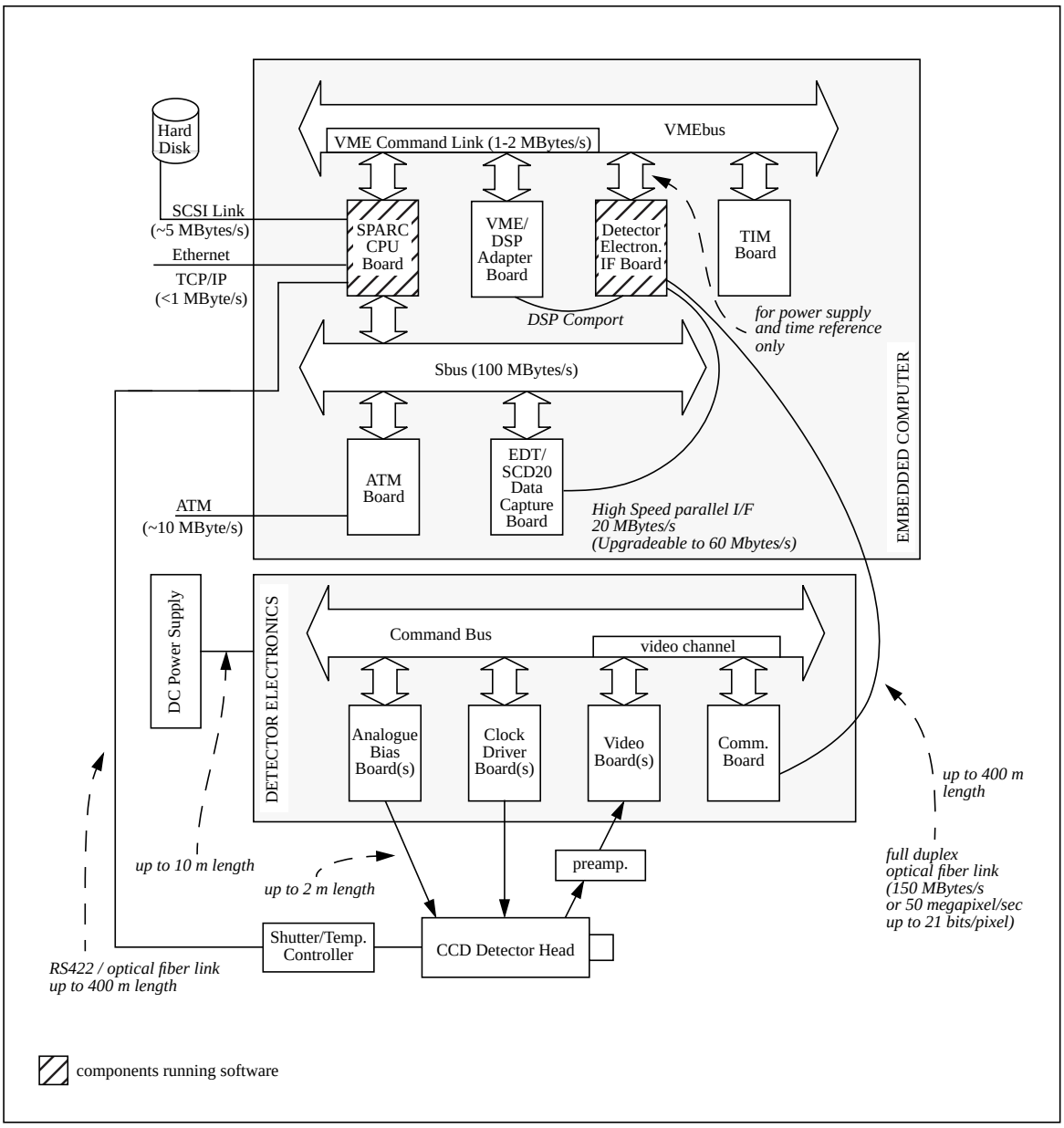

Fig.2 - FIERA Hardware Architecture

Fundamental clock frequency	50 MHz
Number of readout channels	up to 16
Maximum total pixel rate	50 Mps eventually foreseen (10 Mps for 1997)
Number of bits/pixel	up to 21 (initially 16, set by A/D)
Maximum speed per port	5 Mps eventually foreseen (2 Mps for 1997)
Clock drivers	fully programmable (25.6 V swing, 0.1 V resolution, 2 A current)
Number of control bits	virtually unlimited
Analog biases	fully programmable with hardware limits for CCD protection
Gain settings	4
Filtering settings	4 (for different readout rates)
Offset levels	64k levels - each channel individually programmable
Data link	gigabit/sec from detector head to computer (up to 400m long)
Telemetry	all voltages remotely readable
Test signals	Synthetic video generation
Software in the Detector Head	None - all in C, C++ in the Embedded Computer
Modularity	Separate modules allowing upgrades and expandability

Table 1 - FIERA System Specifications

4) **The microsequencer** (extracted from [1])

A significant feature of the FIERA design is the implementation of a **microsequencer** that provides local generation of control bits. This design minimizes the number of high speed signals that are distributed across the detector head electronics backplane. The microsequencer is the key to realization of the high speed multi-level clock drivers and the 256 level synthetic video signal generation.

The main sequencer in FIERA is the Texas Instruments C40 DSP that is on the interface board within the embedded computer. This C40 puts out relatively high level commands to the detector head, such as "*perform a parallel line shift*" or "*read out 1000 pixels*".

These commands are distributed simultaneously to all of the microsequencers that are located in the detector head. The Communication, Clock Driver and Video boards all contain microsequencers (no microsequencer is needed on the Analog Bias board). After receiving a command, the microsequencers output the bit patterns that correspond to the operation requested.

The microsequencer is simply a ***counter circuit combined with a SRAM (static RAM) memory chip***. The counter cycles through address locations and clocks out data from the SRAM. The counter function of the microsequencer is performed by a programmable logic array.

For the microsequencer design to work properly, all microsequencers must work in lock step at all times, since there is no communication between microsequencers. Care must be taken with distribution of the commands and the microsequencer clock, but we have not had significant difficulty in getting this approach to work. The C40 DSP software keeps track of the length of the patterns in the queue and puts out the commands for successive patterns at exactly the correct clock transition. We have tested this operation thoroughly to be certain that successive clock patterns have seamless transitions. One attribute of the microsequencer that makes this task easier is that it has a 2 command buffer at its input.

In order to save memory locations in the SRAM, the clock frequency can be divided to utilize the minimal number of memory locations for storage of each pattern. The microsequencer clock division is performed by loading a register on the communication board. Of course, the microsequencers must finish any previously commanded patterns prior to changing the clock speed. Clock frequencies from 50 MHz to 762 Hz are supported.

5) The software for FIERA

When FIERA operates in standalone mode, all the software runs on the DSPs of the Detector Electronics Interface Board (Parallel C) and on the SPARC CPU (Solaris Operating System, C and C++ programming languages).

When FIERA is being used by an instrument, interface processes run also on the Instrument Workstation (HP or Sun) (see [3] and [4]).

The FIERA Control software communicates with the rest of the VLT Environment through a well defined interface, which is the same for all the VLT instruments (see Fig.3).

This interface consists of (see [5] and [6]):

- commands / replies, using the Message System of the VLT Central Common Software (CCS);
- configuration files, to define the system hardware configuration;
- setup files, to define the exposure parameters;
- image data, delivered as FITS format files;
- logging messages, using the CCS Logging System;
- error messages, using the CCS Error System;

In particular, the software running on the SPARC CPU is responsible for:

1. Control of all phases of an exposure, logging the exposure events (shutter opening, exposure start etc) and the error messages, and updating the system state in the online database (HP-RTAP)
2. Generating of the readout sequences.
3. Reading and reordering of the image pixels.
4. Fast image display via the VLT Real Time Display (RTD).

The software running on the DSPs of the Detector Electronics Interface Board is responsible for:

1. Voltage and clock settings.

2. Performing of actions which have strict real-time constraints, e.g. microsequencer scheduling.
3. Image data flow path control.
4. Interface with programs belonging to other VLT software modules and using real-time image processing results produced by the CCD software. e.g for Adaptive Optics.

Special code which must be instrument specific (real time processing, etc) can be introduced into the system through the use of shared libraries.

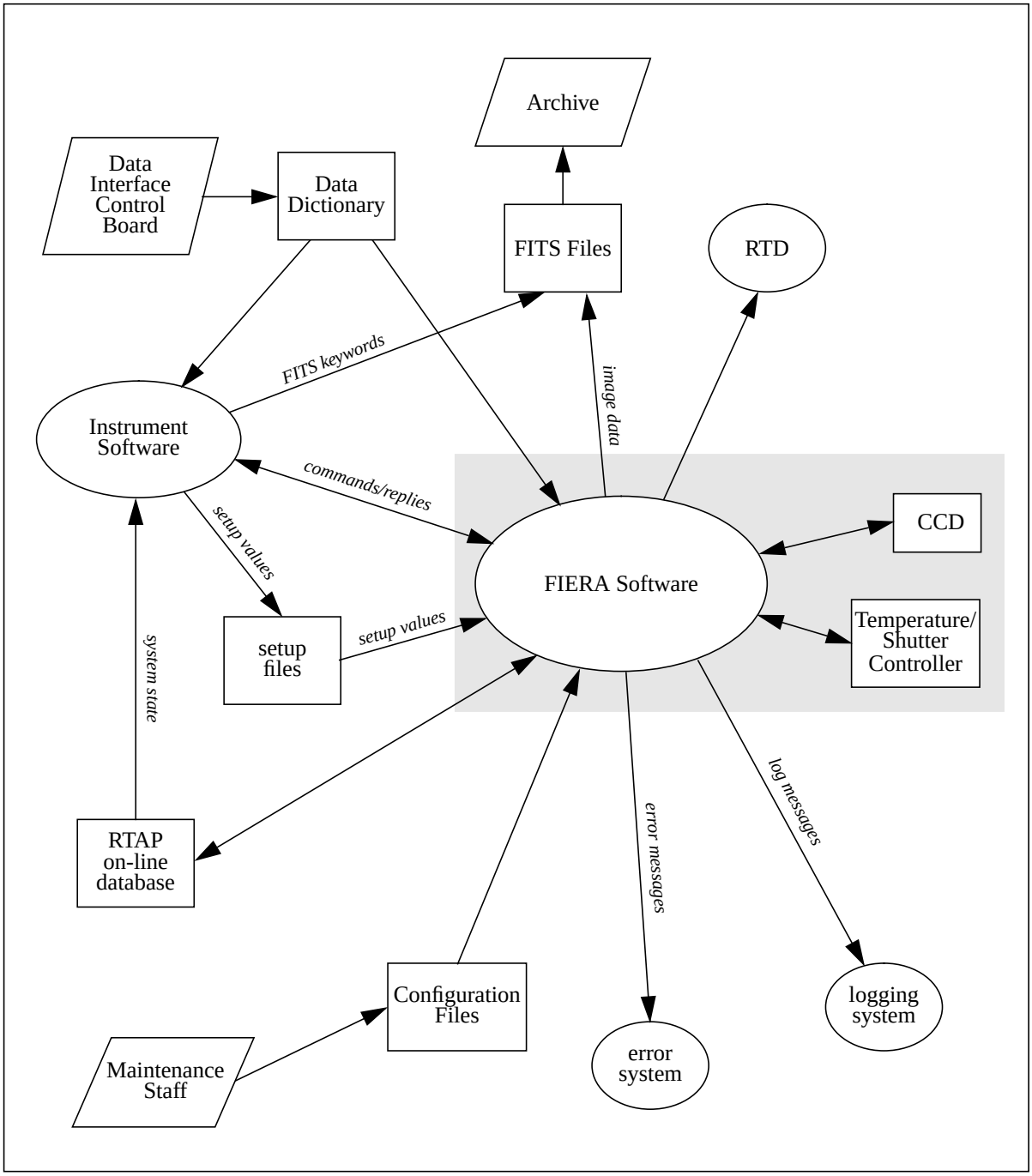

Fig.3 - FIERA Software interface with the VLT environment

6) FIERA performances

The first "***Oktoberfest '96***" prototype of FIERA system has been successfully assembled in October 1996, in the Optical Detector Team laboratories at ESO, Garching.

This prototype has proven the general concept and architecture, and in 1997 FIERA has gone through test and redesign stages.

Table 2 shows the readout performances measured in September 1997 on a MIT/LL 2Kx4K, 15 μm pixel full frame CCD chip:

number of outputs used	2
readout time	40 seconds
readout speed	100 kps/port
readout noise (CCD + preamp + FIERA)	2.3 electrons @ 100 kps
system noise (FIERA alone)	0.3 electrons @ 100 kps
crosstalk (FIERA alone)	1:150000

Table 2 - FIERA performances

A FIERA system has been delivered to EEV in Chelmsford, England, for testing the EEV 16 port adaptive optics CCDs, with a burst readout speed of 1 Mps/port (16 Mps total), where Mps stands for megapixel/sec.

To our knowledge, **this is the first 16 port CCD controller yet made for astronomy.** There are some 16 port CCD controllers being used in military projects, but those systems do not have the noise performance or flexibility of FIERA.

The following **goals** are foreseen:

- for the *1997 version*:

  2 Mps/port (limit set by 16 bits ADC)

  10 Mps total (limit set by Data Capture Board)

- and *eventually*:

  5 Mps/port

  50 Mps total

FIERA will see "first light" at La Silla and Paranal telescopes in early 1998.

7) Bibliography

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[3] Cumani C., Donaldson R., "The Architecture for Two Generations of ESO VLT CCD Controllers", in the proceedings of the "ESO Workshop on Optical Detectors for Astronomy, Garching, October 8-10, 1996" - J.W. Beletic & P. Amico Eds. - Kluwer Academic Publishers

[4] Cumani C., Donaldson R., VLT-SPE-ESO-13640-1266, 1.0, 16/04/97, "FIERA CCD Controller, Software Functional Specifications" (available as compressed postscript file at ftp://te1.hq.eso.org/vlt/pub/doc/fiera_sfs1.0.ps.gz)

[5] G. Filippi, VLT-MAN-ESO-17200-0888, 1.0, 17/08/95, "VLT Common Software - Overview" (available as compressed postscript file at ftp://te1.hq.eso.org/vlt/pub/doc/overview_sum1.0.ps.Z)

[6] CCS Team, VLT-MAN-ESO-17210-0619, 1.7, 30/04/97, "CCS User Manual" (available as compressed postscript file at ftp://te1.hq.eso.org/vlt/pub/doc/ccs_sum1.7.ps.gz)

Other information is available on the Optical Detector Team web pages (http://www.eso.org/odt/)