European Southern Observatory

GIRAFFE
CCD Detector Upgrade To "Carreras" Version 2.0 **VLT-TRE-ESO-13730-4806**

	Name	Date	Signature
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Change Record

Issue/ Revision	Date	Section/Page affected	by	Reason
1	4-Jul-08	All	M. Downing	First issue
1.1	14-Jul-08	8.2.13	M. Downing	Temporary release; update section 8.2.13 Variation of Offset Level in a Sequence of Biases.
2.0	27-May-09	Cover Page	M. Downing	Document number added and final release

List of Abbreviations

ADC	Analog to Digital Converter
ADU	Analog to Digital Unit
ATM	Asynchronous Transfer Mode
BOB	Broker for Observation Blocks
CCD	Charge Coupled Device
CFC	Continuous Flow Cryostat
COM1	Commissioning 1
DSP	Digital Signal Processor
EMI	Electromagnetic Immunity
EPER	Extended Pixel Edge Response
FIERA	Fast Imager Electronic Readout Assembly
Gbps	Gigabit/second
IC-LCU	Instrument Control LCU
ICS	Instrument Control System
kps	kilopixel/port/second
LAN	Local Area Network
LCU	Local Control Unit
LRU	Line Replaceable Unit
Mps	Megapixel/port/second
MTBF	Mean Time Between Failures
MIDAS	Image processing software package
ODT	Optical Detector Team
PRISM	Image processing software package
RTD	Real Time Display
TBD	To Be Defined
WS	Workstation

Table of Contents

1 Introduction and Purpose

This document reports on the upgrade of the detector of GIRAFFE from Bruce to Carreras. Carreras (e2v serial number 06383-13-01) is a CCD44-82 2kx4k and is electrically and mechanical identical to Bruce and thus a plug in replacement. Bruce is a standard silicon (nominal thickness 20μm) CCD44-82 and has a single layer AR coating optimized for the Blue. Carreras (the new detector) is a Deep Depletion (nominal thickness 40μm) CCD44-82-82-1-D42 and has a special custom two layer coating (HfO/SiO2) optimized for broadband QE response.

The upgrade was performed by assembling a new cryostat unit by refurnishing the old UVES blue detector head and CFC cryostat (swap out of service when UVES Blue CCD was upgraded) and installing Carreras. The performance of Carreras was fully characterized in this new system before the GIRAFFE detector head and cryostat was brought to ESO Garching to enable the field lens to be swapped onto the new system.

This document describes the performance of the new system with Carreras installed and any differences or changes made to the system during the upgrade. All additional information can be found in the GIRAFFE Detector Preliminary and Final Design Reviews documents (VLT-TRE-ESO-13740-0000) and the original CCD Detector Systems Detector design and performance report (VLT-TRE-ESO-13730-2765) and will not be repeated in this document.

2 Performance Summary Tables

Table 1: Summary of Performance

Parameter	Specification	Comment
Device	Carreras	
Type Number	CCD44-82-82-1-D42	
Serial Number	06383-13-01	
Pixel Size	15μm	
Number of Pixels	2048 x 4096	
PRNU	< 3% RMS	Wavelength 350-900nm, bandwidth of 5nm, and flat field of 50ke-
Cosmetic Quality	No bad columns or glow areas. One bright pixel else cosmetically clean.	Bright Pixel at [234,3040] affects ~ 8-10 neighbours
Dark Current	< 0.8 e-/pixel/hour @ -125 ºC	
Cosmic hit event rate	3.14 ± 0.18 events/min/cm²	
Vertical Charge Transfer Efficiency	0.9999983	
Horizontal Charge Transfer Efficiency	0.999999	
Linearity	< ±0.5% peak-to-peak	

Table 2: Summary of performance of the scientific read out modes.

Mode	Readout speed [kHz]	Dynamic (ADC limited) [Ke-/pixel]	Conversion Factor [e⁻/ADU]	Readout Noise [e⁻]	Read Out Time (s)
1	**50kpx_1x1_HG**	45	0.69 ± 0.1	2.2 ± 0.1	190
5	**225kpx_1x1_LG**	142	2.35 ± 0.1	4.3 ± 0.1	43
7	**625kpx_1x1_LG**	142	2.4 ± 0.1	5.2 ± 0.1	24

3 CCD dimensions and data format

There were no changes to the CCD dimensions or data format. See GIRAFFE Detector Preliminary and Final Design Reviews documents (VLT-TRE-ESO-13740-0000) for details.

4 GIRAFFE detector – Readout modes

There were no changes to the read out modes. See GIRAFFE Detector Preliminary and Final Design Reviews documents (VLT-TRE-ESO-13740-0000) for details.

5 Bias X/Y Profile

Bias exposures show some ramp-up effect, along the X and Y-axis (Figure 1 to Figure 4) however the shapes are stable from readout to readout (< 1-2 adus). Please see §8.2.13 for discussion of variation of offset level in a sequence of biases where the first bias is slightly different to the rest.
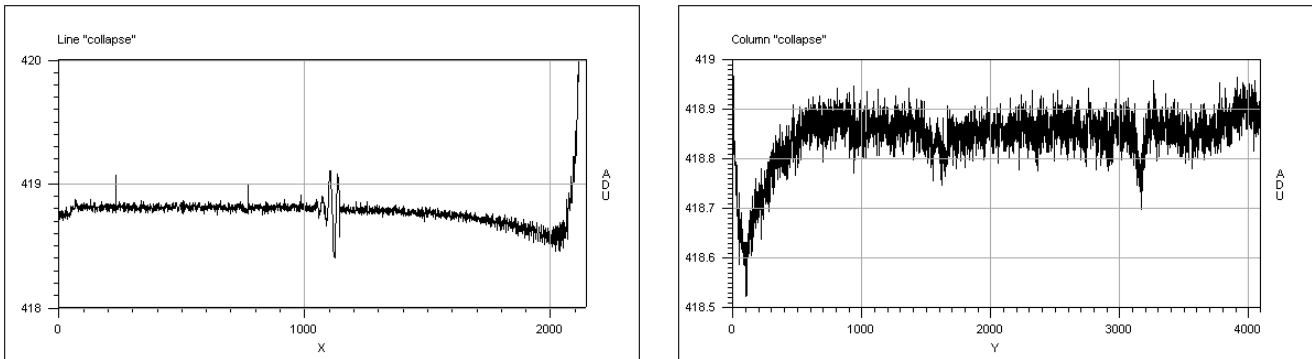

Figure 1: X/Y Bias profile of Carreras in Garching: Left: Row plot of the Median stack of 10 Bias Images (read out mode 225kpx_1x1_HG of gain 0.53e/ADU) collapsed in column. Right: Column plot of the Median stack of 10 Bias Images (read out mode 225kpx_1x1_HG of gain 0.53e/ADU) collapsed in row direction.
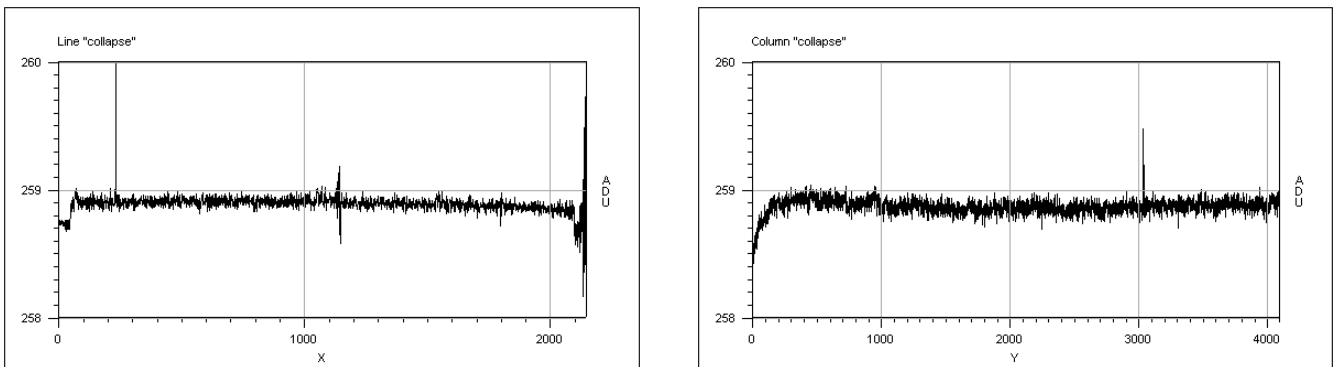

Figure 2: X/Y Bias profile of Carreras in Paranal: Left: Row plot of the Median stack of 5 Bias Images (read out mode 50kpx_1x1_HG of gain 0.69e/ADU) collapsed in column. Right: Column plot of the Median stack of 5 Bias Images (read out mode 50kpx_1x1_HG of gain 0.69e/ADU) collapsed in row direction.
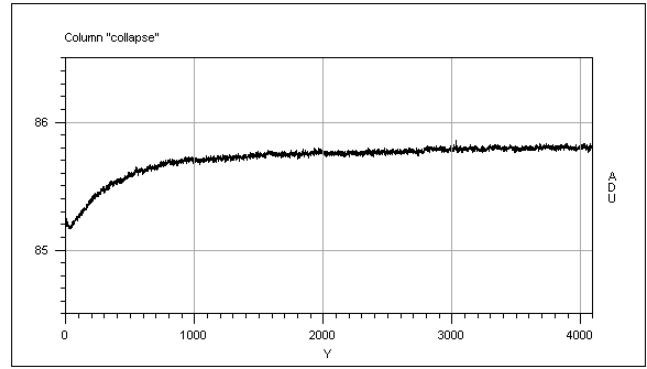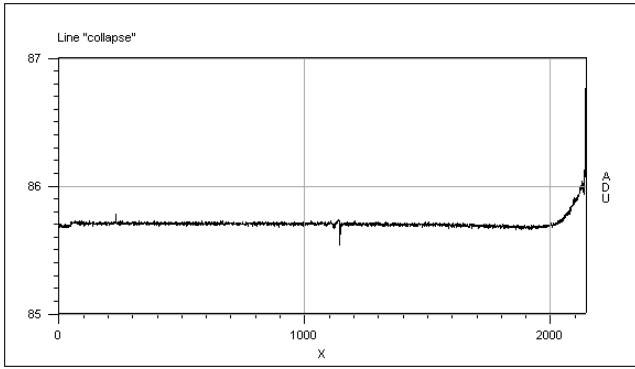
Figure 3: X/Y Bias profile of Carreras in Paranal: Left: Row plot of the Median stack of 10 Bias Images (read out mode 225kpx_1x1_LG of gain 2.35e/ADU) collapsed in column. Right: Column plot of the Median stack of 10 Bias Images (read out mode 225kpx_1x1_LG of gain 2.35e/ADU) collapsed in row direction.

Figure 4: X/Y Bias profile of Carreras measured in Paranal: Left: Row plot of the Median stack of 5 Bias Images (read out mode 625kpx_1x1_LG of gain 2.4e/ADU) collapsed in column. Right: Column plot of the Median stack of 5 Bias Images (read out mode 625kpx_1x1_LG of gain 2.4e/ADU) collapsed in row direction.
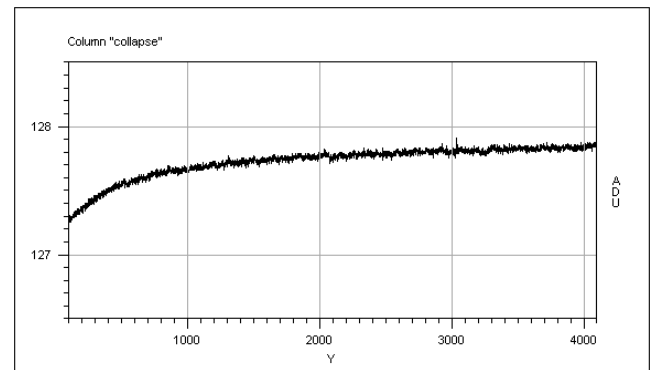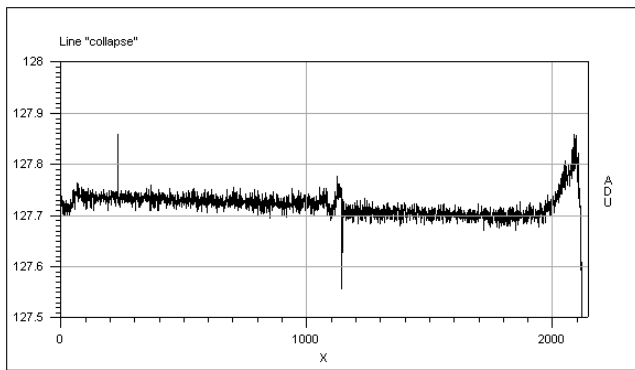
6   Cryogenic parameters

6.1   CCD temperatures

Carreras is operated at the same temperature (see Table 3 that contains important temperatures) as Bruce.

Table 3: Important CCD/Cryostat temperatures.

	Temperature (°Celsius)	Temperature (°Kelvin)	Notes
CCD Table	-127.3	144	**This is set up by the Pulpo.dat file when Fiera starts up.**
Actual CCD temperature	-120	150	There is an offset of 7 degrees between the CCD carrier table and the CCD surface (silicon).
CFC cold plate temperature	-155	123	Set by the CFC controller
Electronic box shut down temp	40	313	Set by Hardware

Figure 5 contains images of two regions at the top (region furthest from the serial register) of a one hour Dark of Carreras showing cosmic rays. The left image is a region at the top left hand side. The right image is a region at the top right hand side. At the selected temperature of 144K, no smearing of the cosmic rays is observed on either side of the CCD thus confirming both good parallel and serial CTE. The image was read out through the right amplifier.
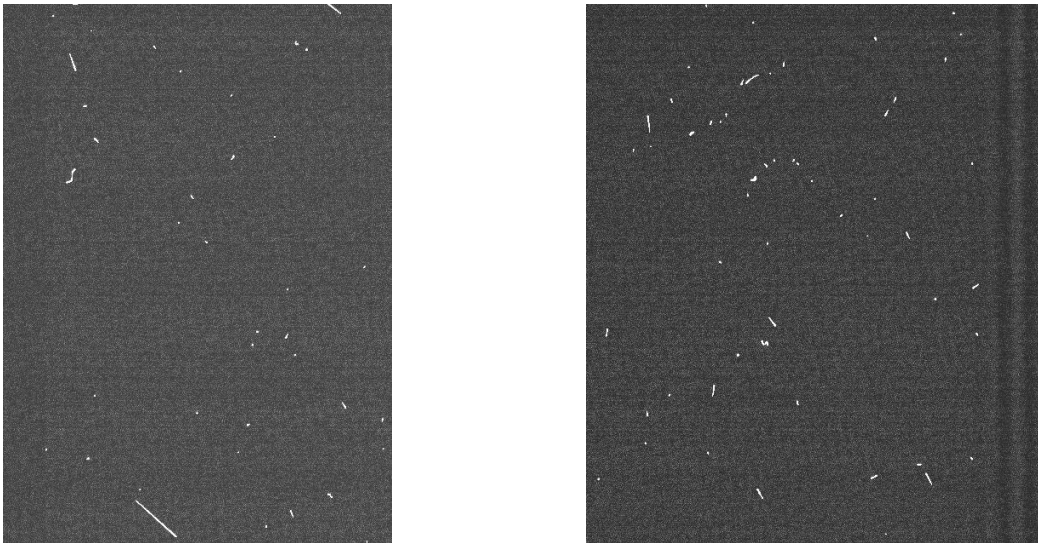
Figure 5: Dark current images at top (region furthest from serial register) of Carrera. Left: Left side of CCD. Right: Right side of CCD. At 144K, no smearing of the cosmic rays are observable on either side at the top of the CCD thus confirming both good parallel and serial CTE.

6.2   Telemetry and alarms

There were no changes to the alarm settings.

7 Fiera detector head electronics and hardware setup

There were no changes to the FIERA hardware. See GIRAFFE Detector Preliminary and Final Design Reviews documents (VLT-TRE-ESO-13740-0000) for details.

7.1 CCD operating voltages

Reset drain, RDR and RDL, and output drain, ODR and ODL, bias voltages were modified (optimized) for Carreras to provide better linearity and read noise. All other voltages were not changed.

The contents of the voltage definition file follows:
$INS_ROOT/SYSTEM/COMMON/CONFIGFILES/CCDNAME$/volttable.def.

```
###############################################################################
#Author :       Cyril CAVADORE
#CAMERA :       Giraffe   ( 1 EEV CCD)
#Purpose:       This is the global voltage definition table
#               European Southern Observatory (ESO)
#Date:          20.11.00
#
###############################################################################
#
#Revision:
#  1  Mark Downing   - Bias voltages ODR, RDR, ODL and RDL modified to suit
#                      upgrade detector Carreras
#
#
###############################################################################
#   GOBAL VOLTAGE DEFINITION TABLE
#
# This table defines the voltages, which will be applied to peripherals
# at initialization time. It also defines the high and low limits, which may
# be set for these voltages
###############################################################################
# BRD_ID  PERIPH_ID           LOW     HIGH    TOLERANCE     INIT_VAL
#
# Anabias voltages are in 0.001 volts
#
###############################################################################
#   BIASBRD 0 is for the EEV CCD-44 in the mosaic
###############################################################################
# BRD_ID  PERIPH_ID           LOW     HIGH    TOLERANCE     INIT_VAL

# CONNECTOR P0 - A
# STANDARD CONFIGURATION FOR EEV44-82 CCDs

# BRD_ID  PERIPH_ID          LOW     HIGH    TOLERANCE     INIT_VAL
BRD_ANABIAS0 ANB_PRESET_VOLT_A    -3500   -1000   10000          -3500 #OG1R
BRD_ANABIAS0 ANB_PRESET_VOLT_B    -2500   -1000   10000          -2500 #OG2R
BRD_ANABIAS0 ANB_PRESET_VOLT_C    20000   26000   10000          22500 #ODR
BRD_ANABIAS0 ANB_PRESET_VOLT_D    11000   15000   10000          10500 #RDR
BRD_ANABIAS0 ANB_PRESET_VOLT_E    20000   26000   10000          25000 #JDR
BRD_ANABIAS0 ANB_PRESET_VOLT_F    20000   26000   10000          25000 #JDL
BRD_ANABIAS0 ANB_PRESET_VOLT_G    10000   23000   10000          18500 #DD
BRD_ANABIAS0 ANB_PRESET_VOLT_H     9000   15000   10000          10500 #RDL
BRD_ANABIAS0 ANB_PRESET_VOLT_I    20000   26000   10000          22500 #ODL
BRD_ANABIAS0 ANB_PRESET_VOLT_J    -2500   -1000   10000          -2500 #OG2L
BRD_ANABIAS0 ANB_PRESET_VOLT_K    -3500   -1000   10000          -3500 #OG1L


#The anabias board also has an opto isolated peripheral

BRD_ANABIAS0 ANB_OPTOOUT        0     32767    4               255


#
###############################################################################
# Clock driver rail voltages are in 0.001 volts
#
###############################################################################
#CLOCKDRIVER BOARD 0 is for the EEV CCD44 in the mosaic
###############################################################################
#
#
# BRD_ID        PERIPH_ID        LOW       HIGH     TOLERANCE   INIT_VAL
#
#   CONNECTOR PO-A
#
```

```
BRD_CLKDRV0 CLKDRV_DAC0_LO     -6000     -5000     1000     -5000 #SWL
BRD_CLKDRV0 CLKDRV_DAC0_HI      5000      6000     1000      5000
BRD_CLKDRV0 CLKDRV_DAC1_LO     -6000     -5000     1000     -5000 #SWR
BRD_CLKDRV0 CLKDRV_DAC1_HI      5000      6000     1000      5000
BRD_CLKDRV0 CLKDRV_DAC2_LO     -6000     -5000     1000     -6000 #RF3
BRD_CLKDRV0 CLKDRV_DAC2_HI      5000      6000     1000      6000
BRD_CLKDRV0 CLKDRV_DAC3_LO     -6000     -5000     1000     -6000 #RF2L
BRD_CLKDRV0 CLKDRV_DAC3_HI      5000      6000     1000      6000
BRD_CLKDRV0 CLKDRV_DAC4_LO     -6000     -5000     1000     -6000 #RF1L
BRD_CLKDRV0 CLKDRV_DAC4_HI      5000      6000     1000      6000
BRD_CLKDRV0 CLKDRV_DAC5_LO     -6000     -5000     1000     -6000 #RF2R
BRD_CLKDRV0 CLKDRV_DAC5_HI      5000      6000     1000      6000
BRD_CLKDRV0 CLKDRV_DAC6_LO     -6000     -5000     1000     -6000 #RF1R
BRD_CLKDRV0 CLKDRV_DAC6_HI      5000      6000     1000      6000
BRD_CLKDRV0 CLKDRV_DAC7_LO     -6000     -5000     1000     -6000 #DG
BRD_CLKDRV0 CLKDRV_DAC7_HI      5000      6000     1000      6000
#
#      CONNECTOR PO-B
#
BRD_CLKDRV0 CLKDRV_DAC8_LO    -12000     -4000     1000     -8000 #IF1
BRD_CLKDRV0 CLKDRV_DAC8_HI     -2000      4000     1000      2000
BRD_CLKDRV0 CLKDRV_DAC9_LO    -12000     -4000     1000     -8000 #IF2
BRD_CLKDRV0 CLKDRV_DAC9_HI     -2000      4000     1000      2000
BRD_CLKDRV0 CLKDRV_DAC10_LO   -12000     -4000     1000     -8000 #IF3 Makes the line reset
BRD_CLKDRV0 CLKDRV_DAC10_HI    -2000      4000     1000      2000
BRD_CLKDRV0 CLKDRV_DAC11_LO    -0000     -0000     1000     -0000 #empty
BRD_CLKDRV0 CLKDRV_DAC11_HI     0000      0000     1000      0000
BRD_CLKDRV0 CLKDRV_DAC12_LO    -6000     -4000     1000     -6000 #FRL
BRD_CLKDRV0 CLKDRV_DAC12_HI     6000      8000     1000      6000
BRD_CLKDRV0 CLKDRV_DAC13_LO    -6000     -4000     1000     -6000 #FRR
BRD_CLKDRV0 CLKDRV_DAC13_HI     6000      8000     1000      6000



#
# Gain should be interpreted as follows
# There are two gains, gain1 is on the preamp, gain2 is on the video board.

# Gain1 =
#     3 == 1.5
#     1 == 2.25
#     0 == 3.0
#
# Gain2 =
#     0 = Minimum (2.5)
#     1 = Maximum (12.5)
#
# INIT VALUES, overridden by modes files,  High_gain_filtre_xxx.volt
# or Low_gain_filtre_xxx.volt


# BRD_ID  PERIPH_ID          LOW    HIGH   TOLERANCE    INIT_VAL

BRD_VIDBRD0 VID_GAIN1_CHAN0      0      3       0            1
BRD_VIDBRD0 VID_GAIN1_CHAN1      0      3       0            1
BRD_VIDBRD0 VID_GAIN1_CHAN2      0      3       0            1
BRD_VIDBRD0 VID_GAIN1_CHAN3      0      3       0            1

BRD_VIDBRD0 VID_GAIN2_CHAN0      0      1       0            0
BRD_VIDBRD0 VID_GAIN2_CHAN1      0      1       0            0
BRD_VIDBRD0 VID_GAIN2_CHAN2      0      1       0            0
BRD_VIDBRD0 VID_GAIN2_CHAN3      0      1       0            0

BRD_VIDBRD0 VID_FILT_CHAN0       0      3       0            0
BRD_VIDBRD0 VID_FILT_CHAN1       0      3       0            0
BRD_VIDBRD0 VID_FILT_CHAN2       0      3       0            0
BRD_VIDBRD0 VID_FILT_CHAN3       0      3       0            0

BRD_VIDBRD0 VID_TESTVID_CHAN0    0      1       0            0
BRD_VIDBRD0 VID_TESTVID_CHAN1    0      1       0            0
BRD_VIDBRD0 VID_TESTVID_CHAN2    0      1       0            0
BRD_VIDBRD0 VID_TESTVID_CHAN3    0      1       0            0

#
# Video Offsets are in 0.001 volts
#
# BRD_ID  PERIPH_ID          LOW    HIGH   TOLERANCE    INIT_VAL
#
# Overridden by *volt files, just for INIT

BRD_VIDBRD0 VID_OFFSET_CHAN0     0    65535    6553         0
BRD_VIDBRD0 VID_OFFSET_CHAN1     0    65535    6553         0
BRD_VIDBRD0 VID_OFFSET_CHAN2     0    65535    6553         0
BRD_VIDBRD0 VID_OFFSET_CHAN3     0    65535    6553         0
```

Giraffe CCD Detector Upgrade to "Carreras"
VLT-TRE-ESO-13730-4806

8 CCD system performance data

8.1 Gain and readout noise

The following table shows noise/gain figures measured in February 2008 at Garching HQ during detector characterization on the ODT Test Bench.

Mode	Readout speed [kHz]	Dynamic (ADC limited) [Ke-]	Readout port	Conversion factor [e⁻/ADU]	Readout noise [e⁻]
1	50kpx_1x1_HG	38	Left or Right	0.58 ± 0.05	1.95 ± 0.1
2	50kpx_1x2_HG	38	Left or Right	0.58 ± 0.05	1.95 ± 0.1
3	225kpx_1x1_HG	35	Left or Right	0.53 ± 0.05	3.1 ± 0.1
4	225kpx_1x2_HG	35	Left or Right	0.53 ± 0.05	3.1 ± 0.1
5	225kpx_1x1_LG	157	Left or Right	2.4 ± 0.05	4.3 ± 0.1
6	225kpx_1x2_LG	157	Left or Right	2.4 ± 0.05	4.3 ± 0.1
7	625kpx_1x1_LG	157	Left or Right	2.4 ± 0.05	5.0 ± 0.1

The following table shows noise/gain figures measured in April 2008 at Garching HQ during final detector characterization of upgrade system with Giraffe video and bias boards installed in the ODT Test Bench FIERA.

Mode	Readout speed [kHz]	Dynamic (ADC limited) [Ke-]	Readout port	Conversion factor [e⁻/ADU]	Readout noise [e⁻]
1	50kpx_1x1_HG	45	Left or Right	0.7 ± 0.05	2.2 ± 0.1
2	50kpx_1x2_HG	45	Left or Right	0.7 ± 0.05	2.2 ± 0.1
3	225kpx_1x1_HG	41	Left or Right	0.63 ± 0.05	3.1 ± 0.1
4	225kpx_1x2_HG	41	Left or Right	0.63 ± 0.05	3.1 ± 0.1
5	225kpx_1x1_LG	142	Left or Right	2.4 ± 0.05	4.2 ± 0.1
6	225kpx_1x2_LG	142	Left or Right	2.4 ± 0.05	4.2 ± 0.1
7	625kpx_1x1_LG	142	Left or Right	2.4 ± 0.05	5.0 ± 0.1

The following table shows noise figure measured 4-6th May 2008, at Paranal during the upgrade.

Mode	Readout speed [kHz]	Dynamic (ADC limited) [Ke-]	Readout port	Conversion factor [e⁻/ADU]	Readout noise [e⁻]
1	50kpx_1x1_HG	45	Right	0.68 ± 0.1	2.2 ± 0.1
2	50kpx_1x2_HG	45	Right		
3	225kpx_1x1_HG	41	Right	0.63 ± 0.1	3.1 ± 0.1
4	225kpx_1x2_HG	41	Right		
5	225kpx_1x1_LG	142	Right	2.3 ± 0.1	4.3 ± 0.1
6	225kpx_1x2_LG	142	Right		
7	625kpx_1x1_LG	142	Right	2.4 ± 0.1	5.2 ± 0.1

8.1.1 Problem of measuring/calculating gain

The gain is normally determined by taking a progressive increasing time series of two flats at constant illumination and calculating the slope (the measured gain) of the variance versus signal level. It has been

shown previously ("CCD riddle: a) signal vs time: linear; b) signal vs variance: non-linear", M Downing et al, SPIE2006) that e2v CCDs do not have a linear relationship between variance and signal level and thus the gain calculated (Figure 6) by this method is dependent on the signal levels used. The true gain is where the gain curve crosses the Y-axis.
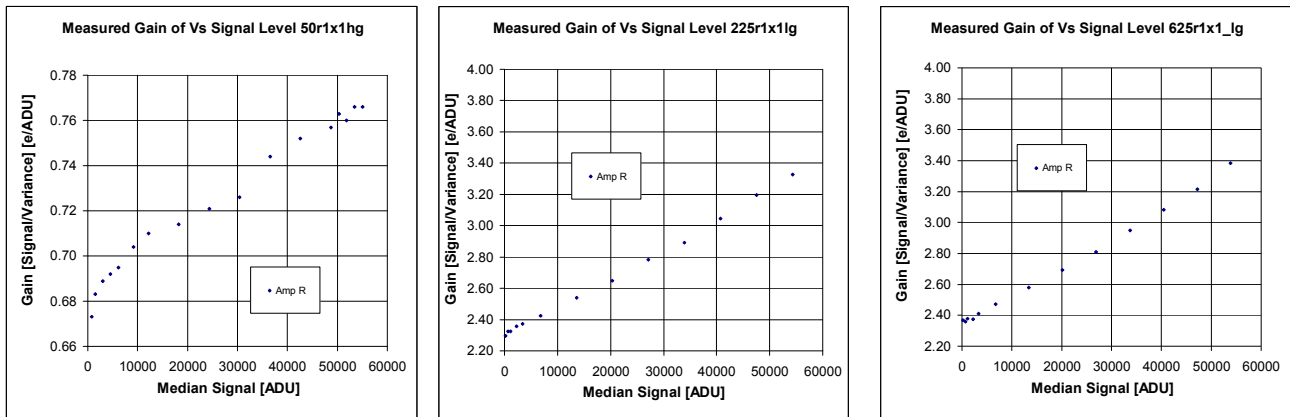

Figure 6: Plots of gain measured using photon transfer curve technique versus signal level. Data taken, 4-6th May 2008, at Paranal during the upgrade. Left: Read out mode 1 (50kpx_1x1_HG). Middle: Read out mode 3 (225kpx_1x1_LG). Right: Read out mode 3 (625kpx_1x1_LG).

8.2   The scientific CCD (Carreras)

8.2.1   CCD specification

CCD serial number   :   06383-13-01
CCD alias name   :   CARRERAS
Type   :   EEV CCD-44 Back Illuminated custom 2-layer AR coated
Number of pixels   :   [H] 2048 [V] 4102
Number of outputs   :   2
Pixel size   :   15x15 μm
Channel potential voltage   :   Not provided by e2v.
Intrinsic pixel full-well   :   150Ke-

8.2.2 Cosmetic defects

Table 4: Carreras cosmetic defect table. Pixel locations are defined w.r.t. image area and 49 needs to be added for the overscan region if the image has not been trimmed of overscan.

<table>
<tr><td colspan="3" align="center">Cosmetic defects table</td></tr>
<tr><td colspan="2"><u>Low level flat field</u></td><td></td></tr>
<tr><td colspan="2"></td><td>Mean number of electrons per pixel ≈ 1000</td></tr>
<tr><td>Type of defect</td><td>Location (x,y)</td><td>Number of pixels affected</td></tr>
<tr><td>Dark pixels (<50% of local mean)</td><td>[623:625,187:188], [661,260], [761:762,3290:3291],[875,1552:1553], [1112,648], [1281:1294,700:705], [1351:3578], [1523:1524, 1378,1379], [1588 ,1508], [1750,198:206], [1766,1073], [1889,2737], [1892,2082].</td><td>Total of 62 pixels (single and clusters of pixels). Most appear to be results of dust particles. Definition: Dark pixel has less than 50% of local mean.</td></tr>
<tr><td>Hot pixels (>20% of local mean)</td><td>None</td><td></td></tr>
<tr><td colspan="2"><u>Bias image</u></td><td>10 exp. of 0 sec dark exposure</td></tr>
<tr><td>Type of defect</td><td>Location (x,y)</td><td>Number of pixels affected</td></tr>
<tr><td>Hot pixels</td><td>None</td><td></td></tr>
<tr><td colspan="2"><u>1 hour dark images</u></td><td>10 exp. of 36000 sec each</td></tr>
<tr><td>Kind of defect</td><td>Location X,Y</td><td>Number of pixels affected</td></tr>
<tr><td>Hot pixels (> 100e/pix/hr)</td><td>[185,3040]</td><td>1</td></tr>
</table>

8.2.3 Bright Pixel

After the Giraffe flange was fitted to the upgrade cryostat in Garching and the system cooled, the bright pixel at [185,3040] was noticed to be much brighter and to affect surrounding pixels. The dependency of the bright pixel with temperature was investigated. As shown in Figure 7, Figure 8, and Figure 9, the intensity of the bright pixel is very dependent on temperature and its effect can be reduced by lowering the detector temperature.

With lower temperatures the serial CTE deteriorates. See Figure 10 showing overscan row plots of flat field images of 26000ADU in mode 3 (225kpx_1x1_HG) for detector temperatures of -120ºC, -125ºC, -130ºC, and -133ºC. The CTE versus temperature was measured using EPER method mode 3 (225kpx_1x1_HG). The results in Table 5 show that the goal specification of serial CTE = 0.999995 can be meet at temperatures as low as -133°C; the lowest possible detector temperature and only achievable with the detector heater fully turned off. As some head room is required for temperature regulation, the detector will be operated at -125°C (the same temperature as Bruce) and if the bright pixels become unmanageable, ways of reducing the detector temperature (e.g. lowering the cold plate temperature) will be investigated.
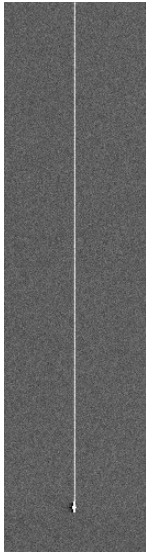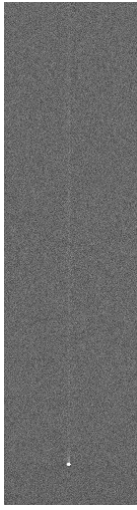
	230	231	232	233	234	235	236	237
3060	450	450	451	450	463	451	449	450
3059	450	450	451	453	465	450	451	451
3058	451	451	450	452	463	451	450	451
3057	450	448	449	452	464	452	450	451
3056	450	451	452	451	462	449	451	450
3055	451	450	452	451	463	451	451	451
3054	451	450	449	453	461	451	452	449
3053	449	452	450	451	462	450	451	451
3052	451	450	451	451	460	451	452	451
3051	451	451	451	453	466	452	451	450
3050	452	449	450	452	460	451	451	451
3049	450	451	451	453	464	450	449	454
3048	451	450	451	454	461	451	449	451
3047	449	450	450	453	469	452	453	449
3046	450	451	451	454	472	450	451	451
3045	451	450	453	493	12247	449	451	450
3044	448	446	438	503	32767	447	451	452
3043	447	444	438	506	32767	449	448	450
3042	448	444	438	519	32767	454	450	451
3041	449	444	492	32767	32767	455	449	448
3040	439	431	481	32767	32767	4852	449	450
3039	446	444	464	7122	32767	450	453	453
3038	449	446	437	495	32767	448	451	450
3037	449	443	439	504	32767	448	448	450
3036	448	446	442	500	32767	451	450	448
3035	452	448	451	451	450	450	448	451

Figure 7: Bright cluster at (3040, 234) at -125°C during the cool down in Garching after mounting the Giraffe front flange.
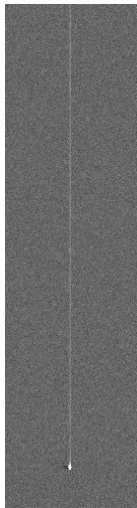
	230	231	232	233	234	235	236	237
3047	448	450	449	452	453	449	449	449
3046	451	451	448	453	454	449	450	452
3045	448	449	450	455	456	450	449	449
3044	451	449	450	455	458	449	448	448
3043	449	450	451	456	463	450	448	449
3042	450	451	457	574	32767	450	451	451
3041	447	446	457	857	32767	448	450	449
3040	446	447	561	32767	32767	794	448	449
3039	448	442	446	622	32767	447	450	451
3038	450	448	455	576	32767	449	449	448
3037	451	449	448	452	448	449	449	448
3036	450	448	450	450	449	450	450	450
3035	450	451	451	449	449	451	449	450

Figure 8: Bright cluster at (3040, 234) at -130°C during the cool down in Garching after mounting the Giraffe front flange.

	230	231	232	233	234	235	236	237
3047	449	451	452	453	454	450	448	449
3046	451	451	453	453	453	450	449	450
3045	451	452	450	454	454	449	450	449
3044	451	451	452	454	453	450	450	450
3043	450	450	451	452	454	452	450	449
3042	449	451	452	454	457	448	450	449
3041	448	451	462	690	32767	449	449	450
3040	450	455	575	18376	32767	465	450	450
3039	448	450	462	662	32767	449	450	450
3038	450	450	449	449	449	447	450	450
3037	452	449	450	449	449	449	450	451
3036	449	450	451	452	450	451	450	450
3035	450	451	449	449	449	449	451	450

Figure 9: Bright cluster at (3040, 234) at -134°C during the cool down in Garching after mounting the Giraffe front flange.
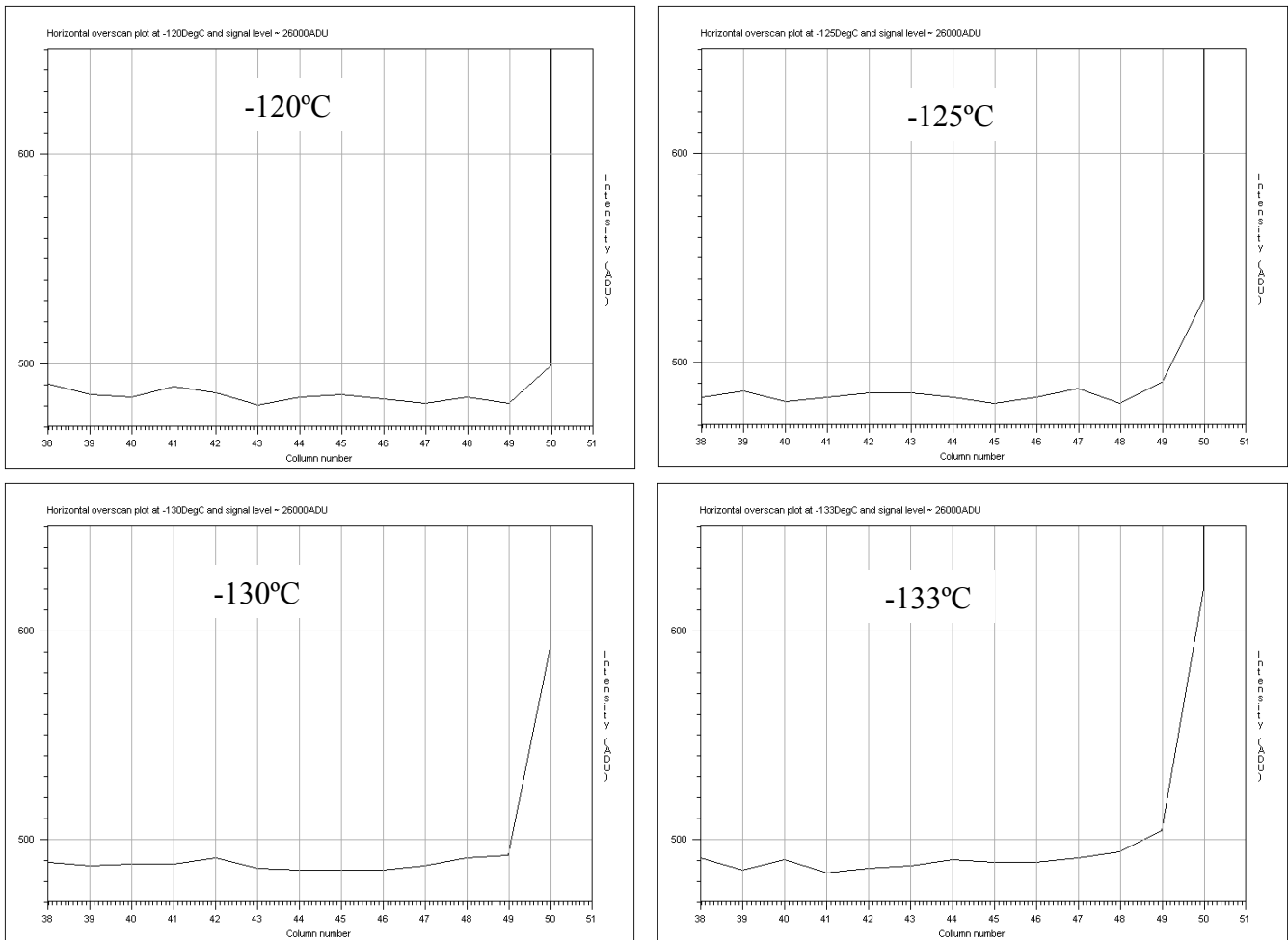
Figure 10: Overscan row plots of flat field images of 26000ADU in mode 3 (225kpx_1x1_HG) (gain of 0.53e/ADU) for detector temperatures of -120ºC, -125ºC, -130ºC, and -133ºC. The first overscan pixel (Pixel 50) has an acceptable amount of deferred charge down to a temperature of -133ºC.

Table 5: Results of serial CTE versus temperature measured using EPER method in read out mode 3 (225kpx_1x1_HG).

CCD Temperature	Serial CTE	Comment
-133°C	0.9999968	
-130°C	0.9999977	
-125°C	0.9999987	
-120°C	0.9999995	

Figure 11 contains the measurement (read out mode 3 225kpx_1x1_LG) at Paranal of the bright pixel at (3040, 234) with final detector temperature of -125°C. The bright pixel affects ~ 10 surrounding pixels.

	232	233	234	235	236	237
3047	89	89	89	88	88	88
3046	87	88	89	89	87	89
3045	88	89	90	88	89	87
3044	88	88	90	88	88	87
3043	89	89	91	88	88	88
3042	88	98	1568	88	88	88
3041	92	166	32767	87	88	87
3040	112	13614	32767	118	87	88
3039	90	131	32767	86	87	89
3038	88	105	6324	87	87	89
3037	87	89	88	88	87	88
3036	88	88	88	87	88	89
3035	88	89	88	88	89	89
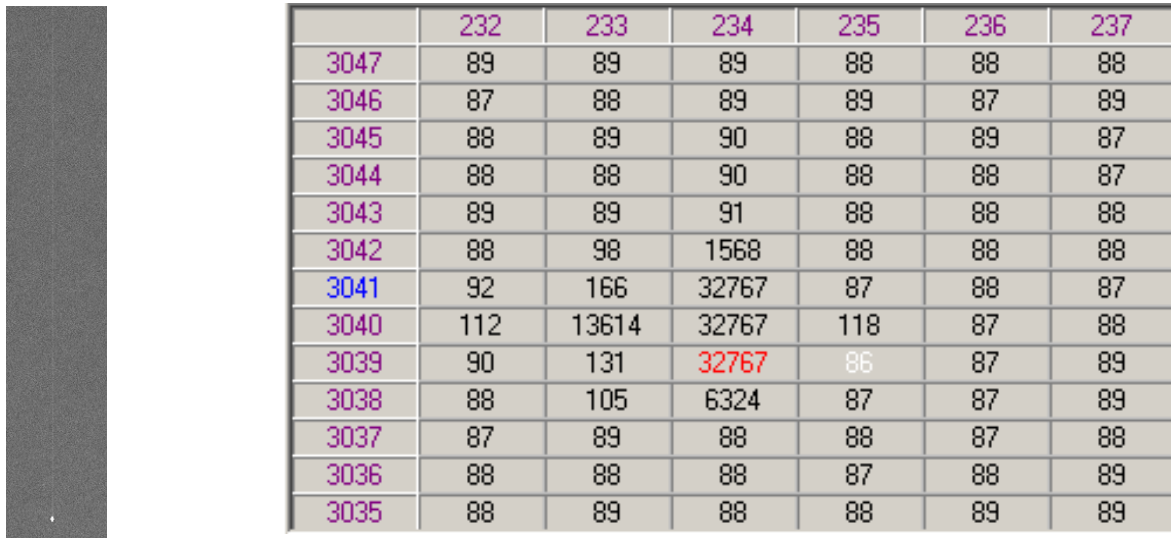
Figure 11: Bright cluster at (3040, 234) at -125°C at Parana in read out mode 5 (225kpx_1x1_LG).

8.2.4 Various Images

The following images (Figure 12 to Figure 16) show full frame images (2x4K) where X=1 and Y=1 are located at the top left of the image. Y is horizontal and increases when going towards right. X is vertical, increasing towards up. The right readout port of the CCD is located at X=2048 and Y=1.
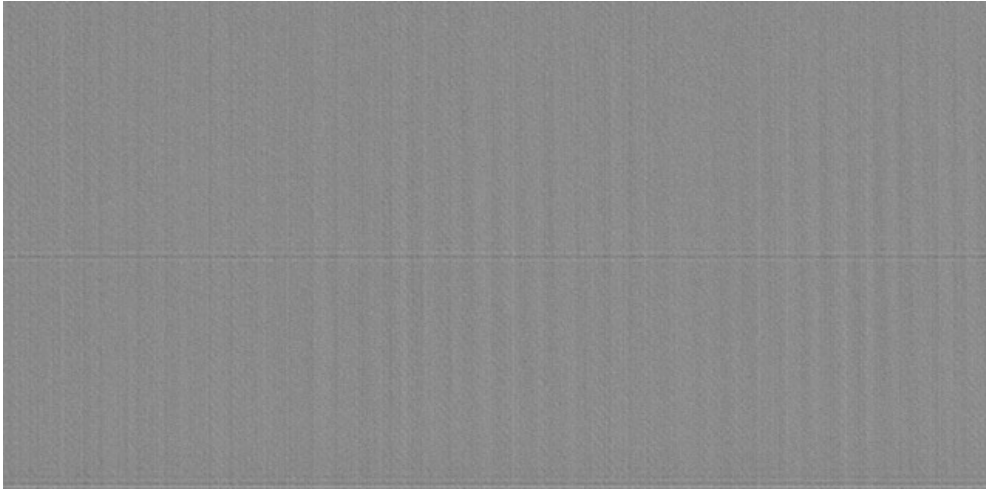
Figure 12: Full frame bias image of upgrade CCD Carreras

Previous CCD
BRUCE

Upgrade CCD
CARRERAS
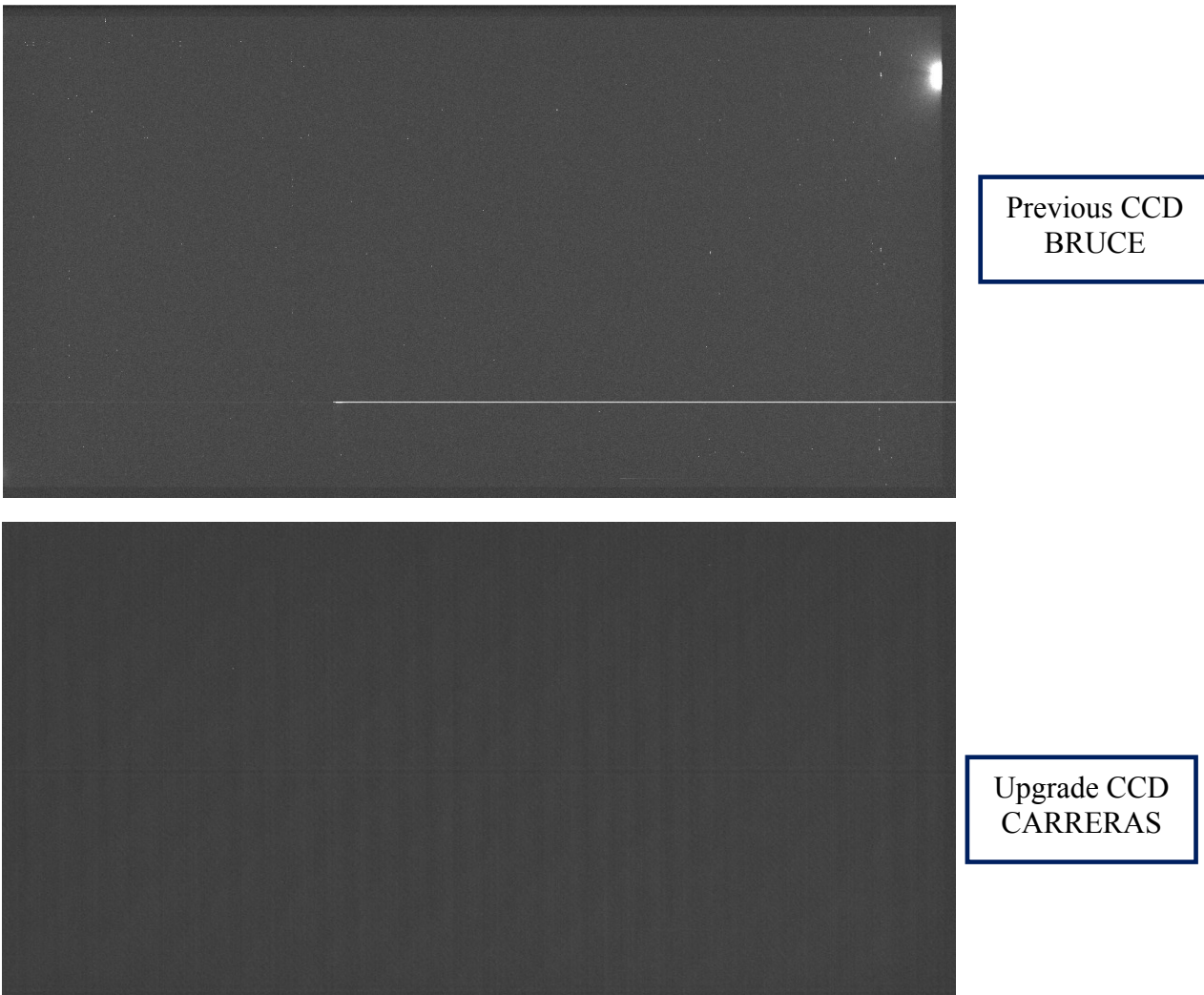
Figure 13: 4x3600s dark exposure median stacked images. Top: Previous CCD Bruce; note the bright column and the amplifier glow in top right hand corner. Bottom: Upgrade CCD Carreras which has only a single hot pixel.
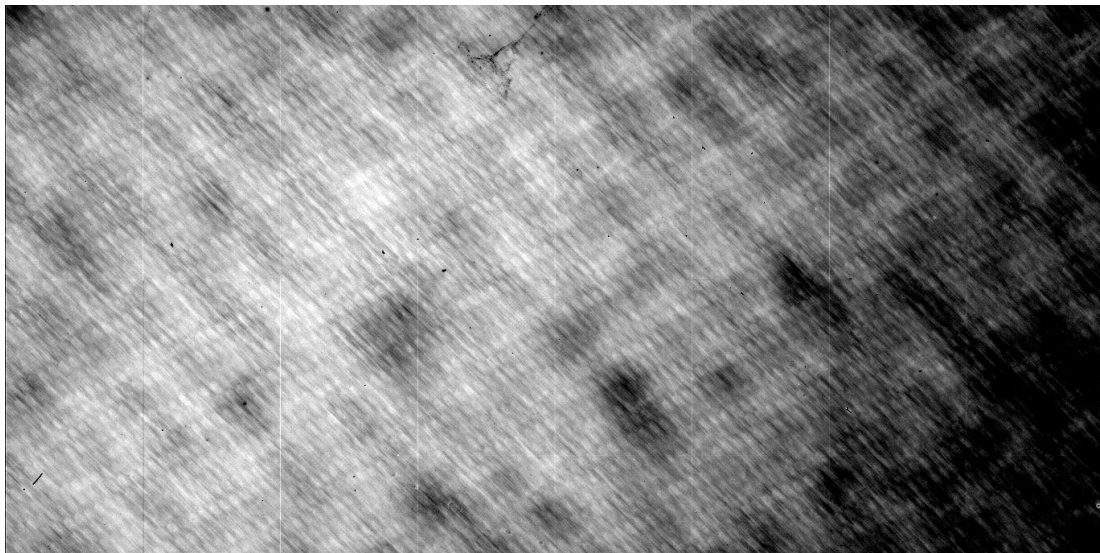
Previous CCD
BRUCE
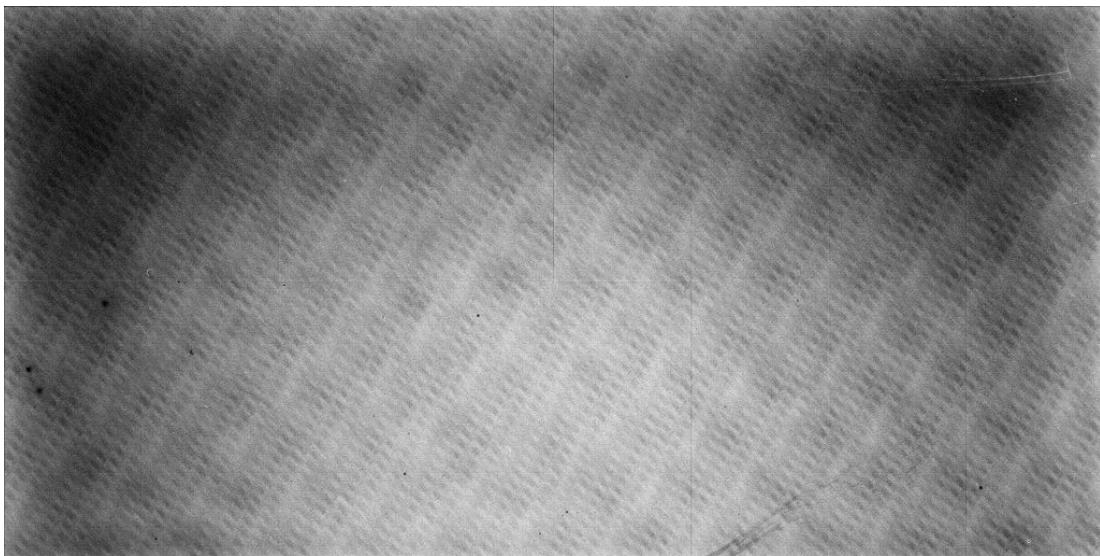
Upgrade CCD
CARRERAS

Figure 14: Comparison of flat field image (~25,000e) at wavelength 350nm and 5nm bandwidth. Top: Previous CCD Bruce. Bottom: Upgrade CCD Carreras. Both CCDs exhibit stitching and laser annealing (diamond) pattern typical of e2v CCDs below 400nm. Patterns are correctable by flat fielding.
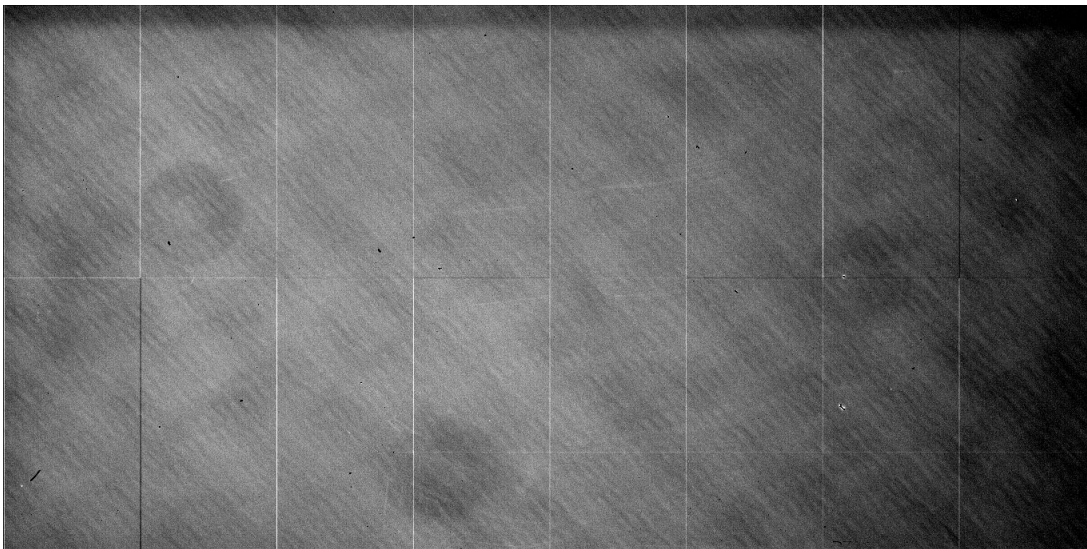
Previous CCD
BRUCE
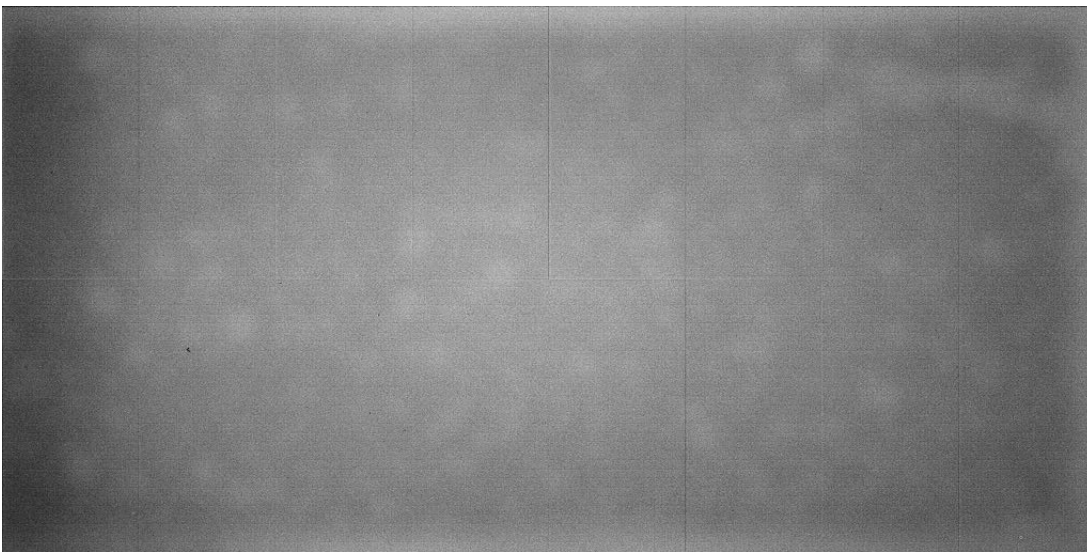
Upgrade CCD
CARRERAS

Figure 15: Comparison of Flat field image (~25,000e) at wavelength 600nm and 5nm bandwidth. Top: Previous CCD Bruce. Bottom: Upgrade CCD Carreras
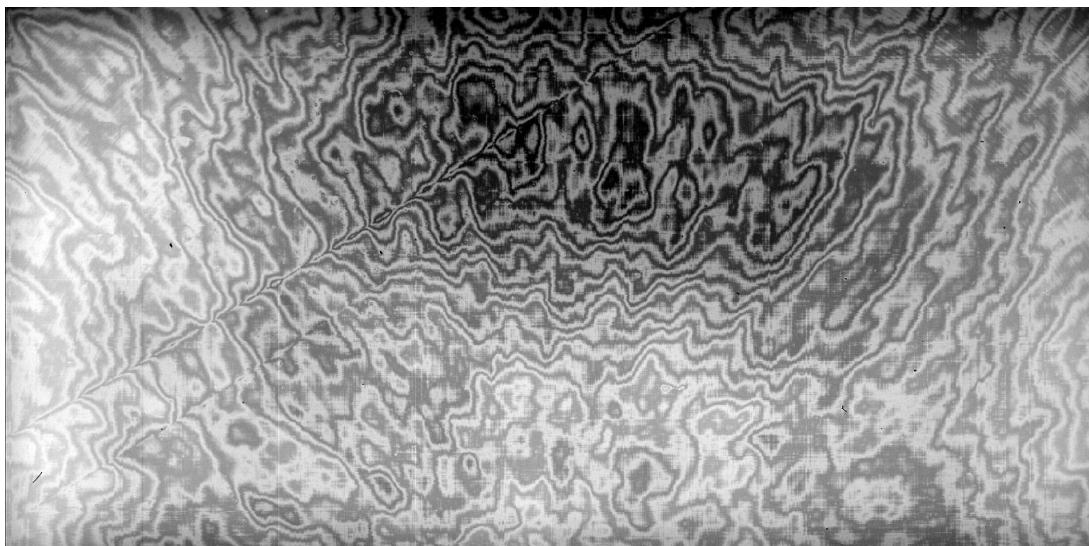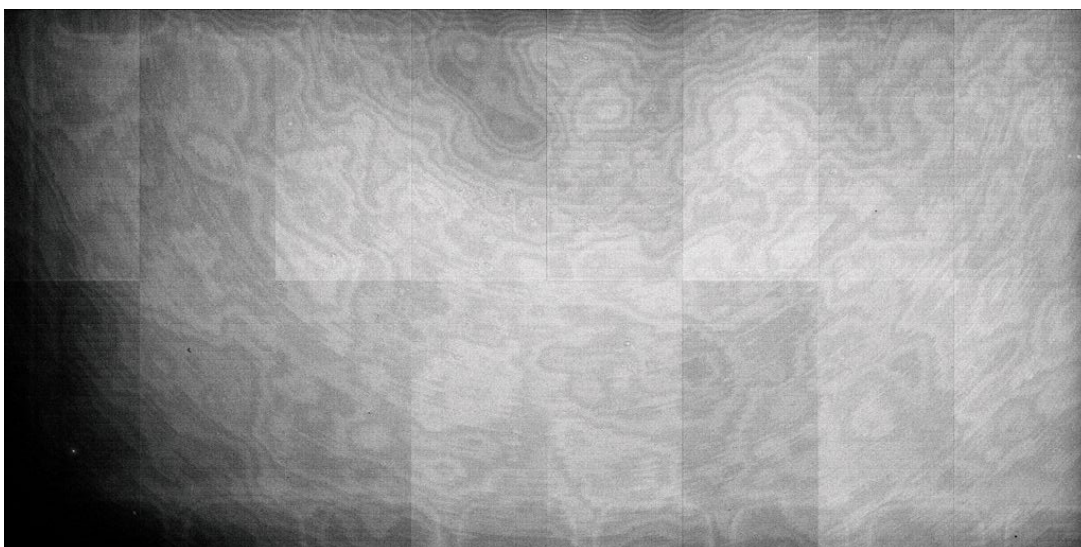
Previous CCD
BRUCE

Upgrade CCD
CARRERAS

Figure 16: Comparison of Flat field images (~25,000e) at wavelength 900nm and 5nm bandwidth. Top: Previous CCD Bruce. Bottom: Upgrade CCD Carreras. Carreras is a much thicker device (40µm versus 20µm) and thus has much less fringing.
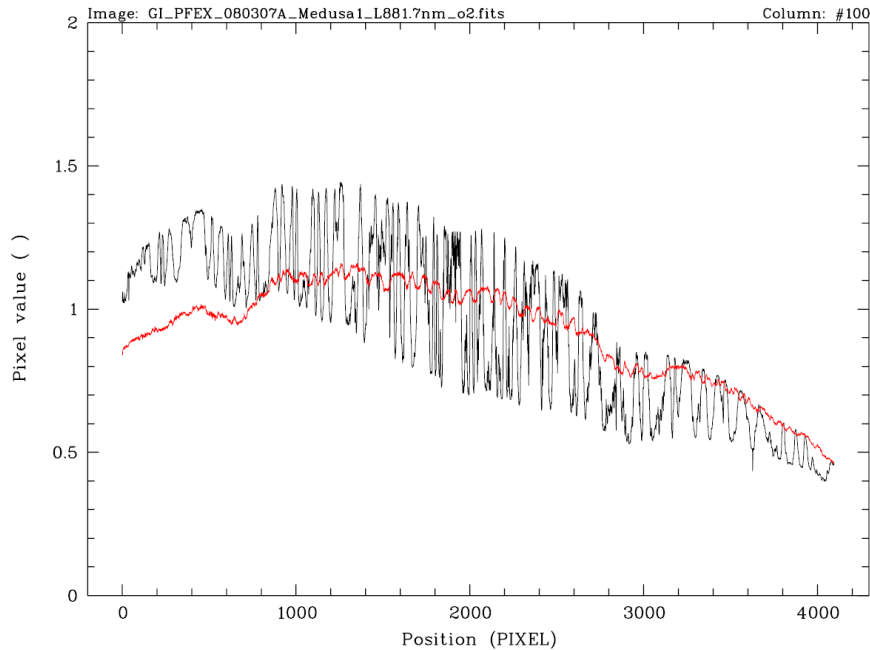
Figure 17: Plot demonstrating the fringing improvement of Carreras (black line) versus Bruce (red line) for Medusa1_L881.7, extracted flat field fibre #100; red.

8.2.5 Dark current

Mean dark current is less than 0.8 e-/pixel/hour @ -125 ºC. Measurement of average dark current is limited by ability to darken the CCD and not the CCD itself. At Paranal, mean dark current less than 2.0 e-/pixel/hour @ -125 ºC was confirmed.

8.2.6 Cosmic ray hit event

Cosmic hit event rate: 1.8 ± 0.04 events/min/cm² in Garching.
Cosmic hit event rate: 3.14 ± 0.18 events/min/cm² at Paranal
At Paranal, the number of pixels affected by cosmics above 10 times the standard deviation is $20{,}000 \pm 1500$ in a one hour dark.

8.2.7 Charge Transfer Efficiency

Vertical CTE to Port A/B (confirmed at Paranal)   : 0.9999983 (five 9s8)
Horizontal CTE to Port A/B (confirmed at Paranal) : 0.999999 (six 9s)

The EPER method was used, at the ESO Garching CCD testbench (and at Paranal) at $-125°C$ in mode 1 (50kpx_1x1_HG).

8.2.8 Linearity

Linearity of both the left and right amplifiers was measured to be better than $\pm 0.5\%$ in the main scientific Mode 5 (225kpx_1x1_LG). All other modes have similar linearity (Figure 18 to Figure 21). Linearity was measure by TDI (Time Domain Integration) method on ODT test bench in Garching while at Paranal linearity was measured by illuminating with stable flat field lamp and increasing exposure. Only readout modes 1, 3, 5, and 7 were measured as modes 1-2, 3-4 and 5-6 are identical.
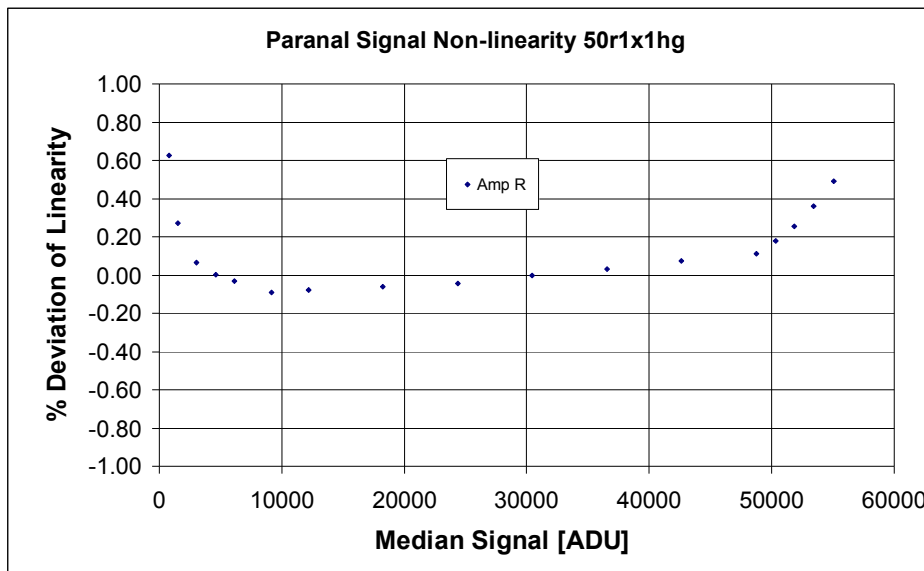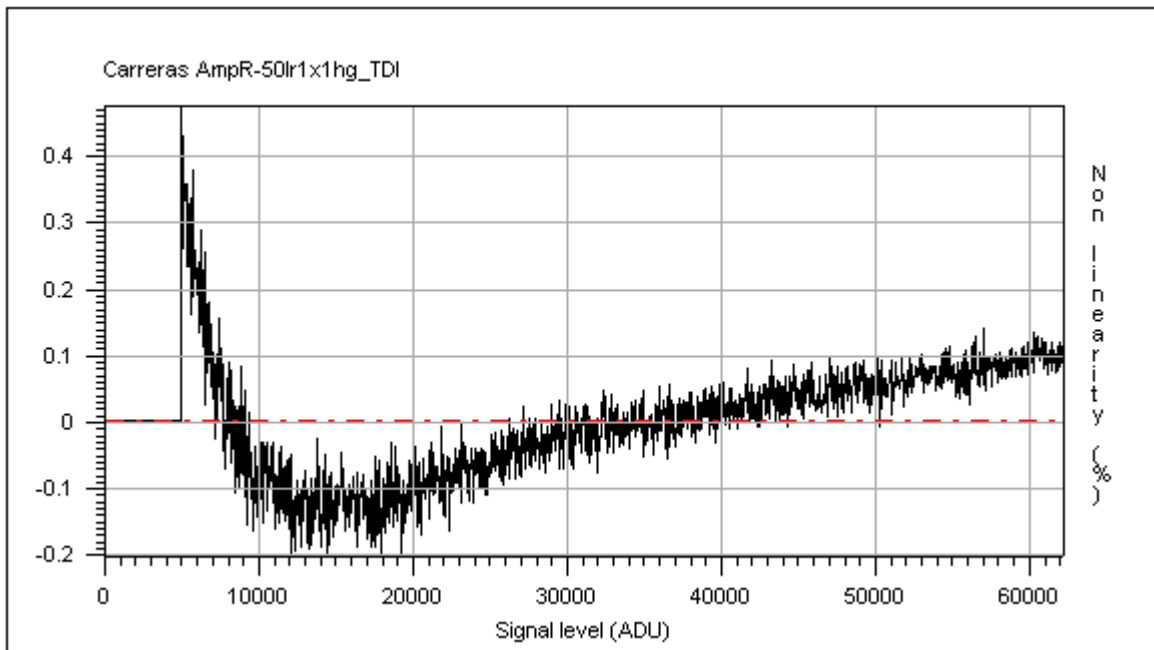
Figure 18: Mode 1 (50kpx_1x1_HG) Non linearity. Top : Plot Non-linearity measured at Garching by TDI method. Bottom: Non-linearity measured at Paranal.
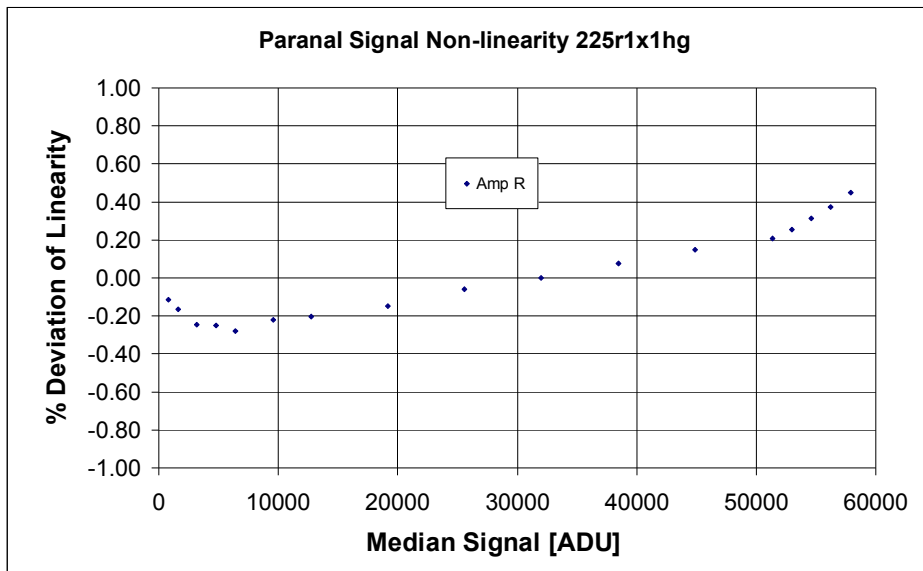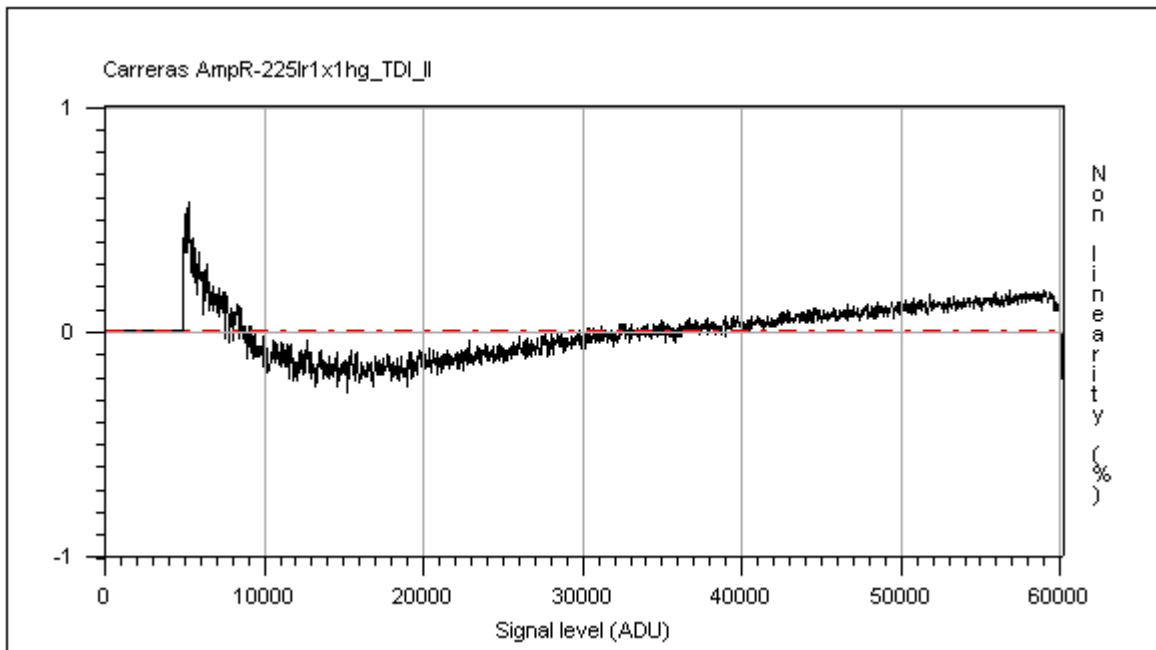
Figure 19: Mode 3 (225kpx_1x1_HG) Non linearity. Top : Plot Non-linearity measured at Garching by TDI method. Bottom: Non-linearity measured at Paranal.
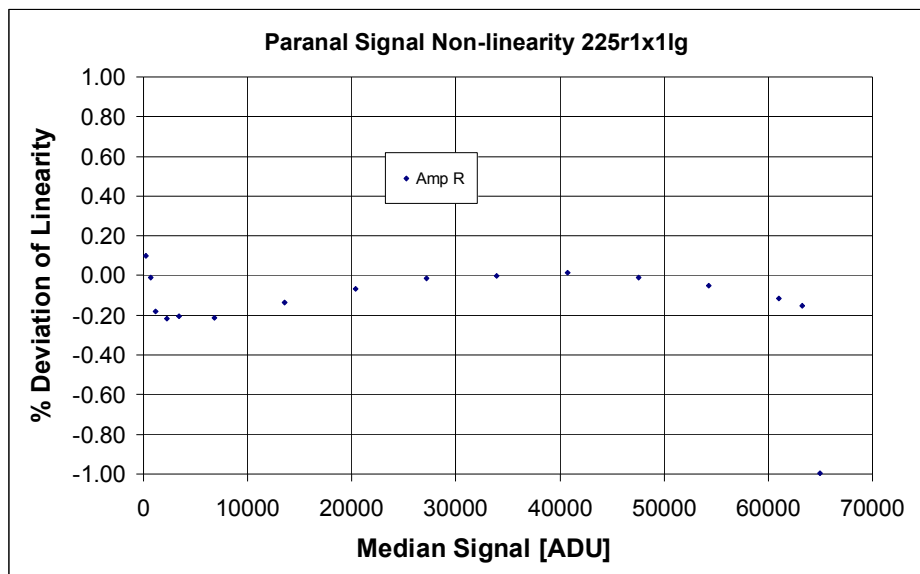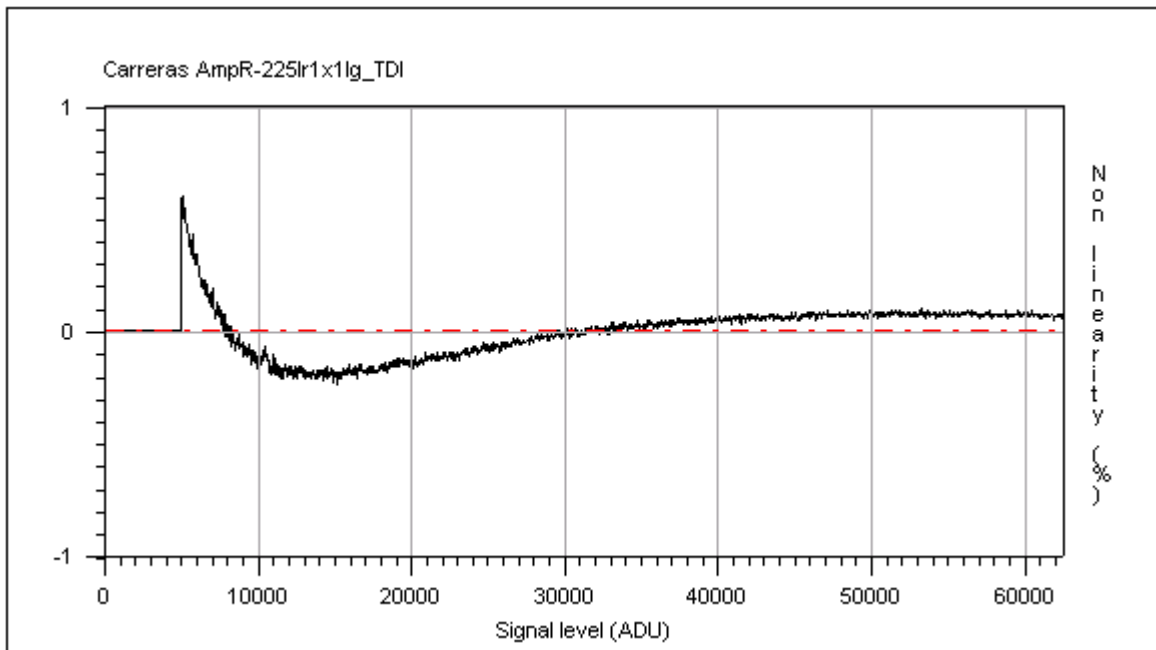
Figure 20: Mode 5 (225kpx_1x1_LG) Non linearity. Top : Plot Non-linearity measured at Garching by TDI method. Bottom: Non-linearity measured at Paranal.
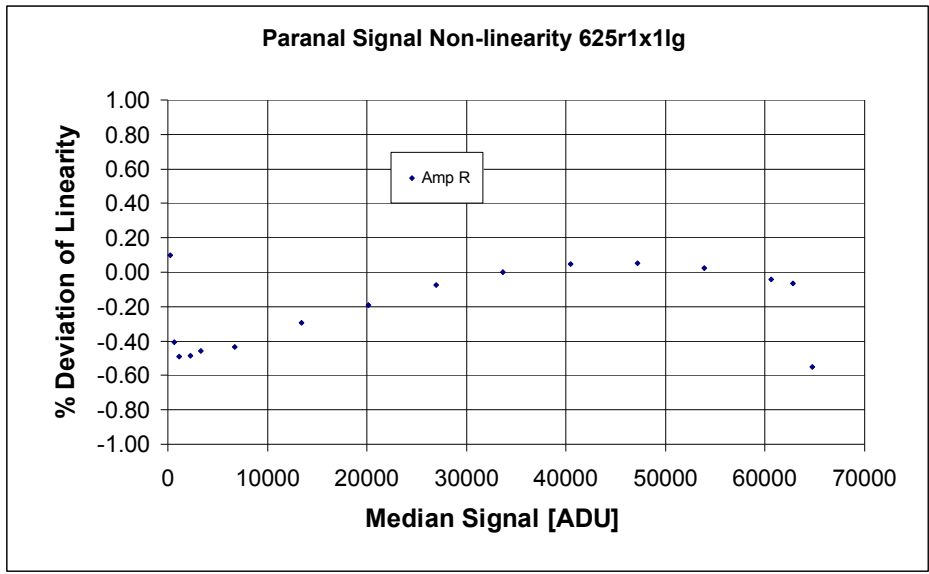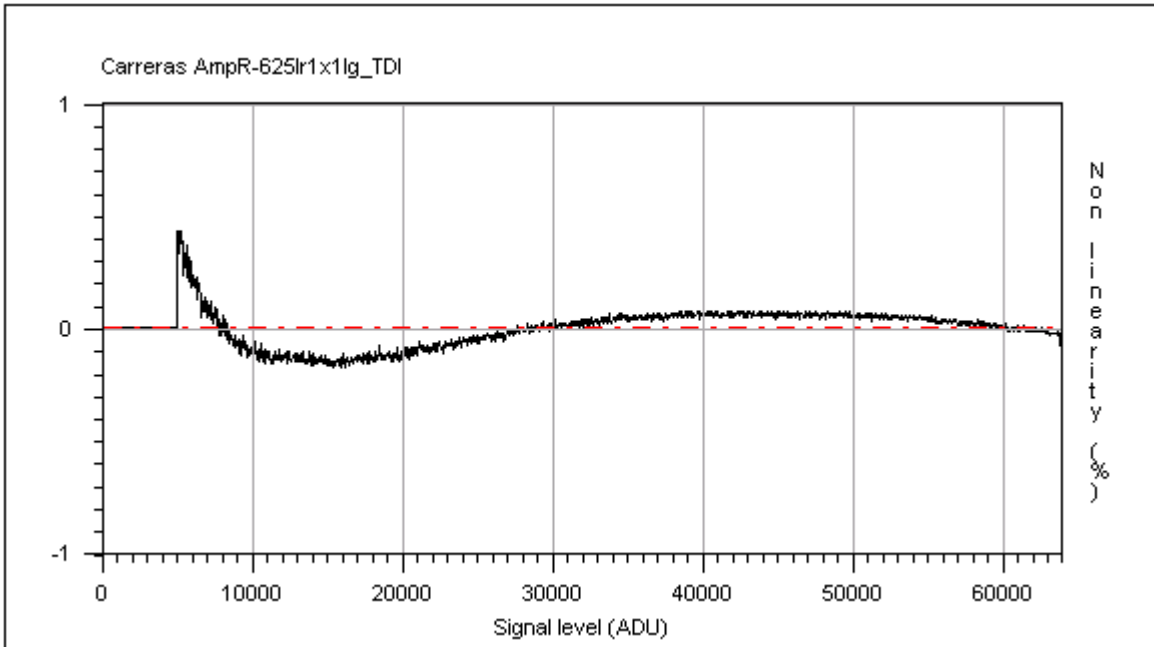
Figure 21: Mode 7 (625kpx_1x1_LG) Non-linearity. Top : Plot Non-linearity measured at Garching by TDI method. Bottom: Non-linearity measured at Paranal.

8.2.9   Readout direction

Toward the right port for ALL modes

8.2.10 CCD flatness

The CCD flatness (Figure 22) was measured at e2v at room temperature. Peak to peak non-flatness is better than specification of < 20 microns.

4K pixels =60mm

-8	-7	-6
-9	-2	-2
-10	-2	0

**2K pixels=
30 mm**
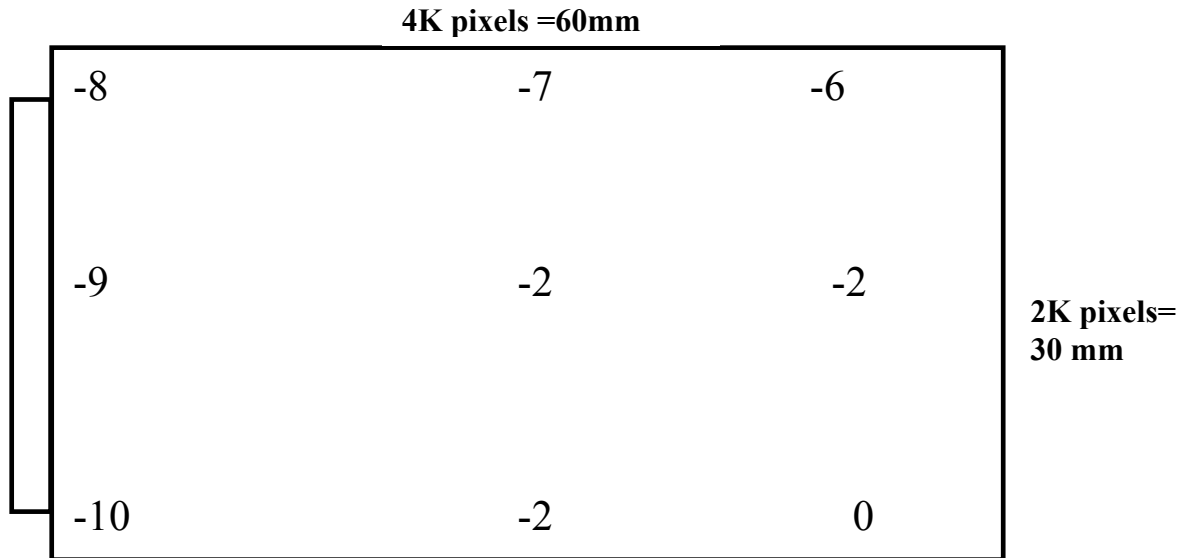
Figure 22: CCD Top view including the deviations in microns from a reference.

8.2.11 Quantum efficiency (QE) and photo-response non uniformity (PRNU)

The QE versus wavelength of both Bruce and Carreras are plotted in Figure 23. The plot (Figure 24) of improvement in QE versus wavelength of Carreras versus Bruce demonstrates one of the reasons why Carreras was chosen. The effective usable bandwidth of GIRAFFE is 370 to 950 nm. At wavelength greater than 370 nm, the QE of Carreras is as good as Bruce in the "blue" and much better in the "red"; reaching 50% improvement at 800 nm and 100% at 900nm.

The plot of PRNU versus wavelength (plotted in Figure 25) of both Bruce and Carreras shows the other reason for the choice of Carreras. While the PRNU of Carreras is a little higher (still much better than required Table 1) in the "blue" than Bruce, it is much lower in the "red". This is due to much lower fringing as Carreras is a much thicker (40 μm) device as it is made on Deep Depletion silicon than Bruce (20 μm) which is made on standard silicon.
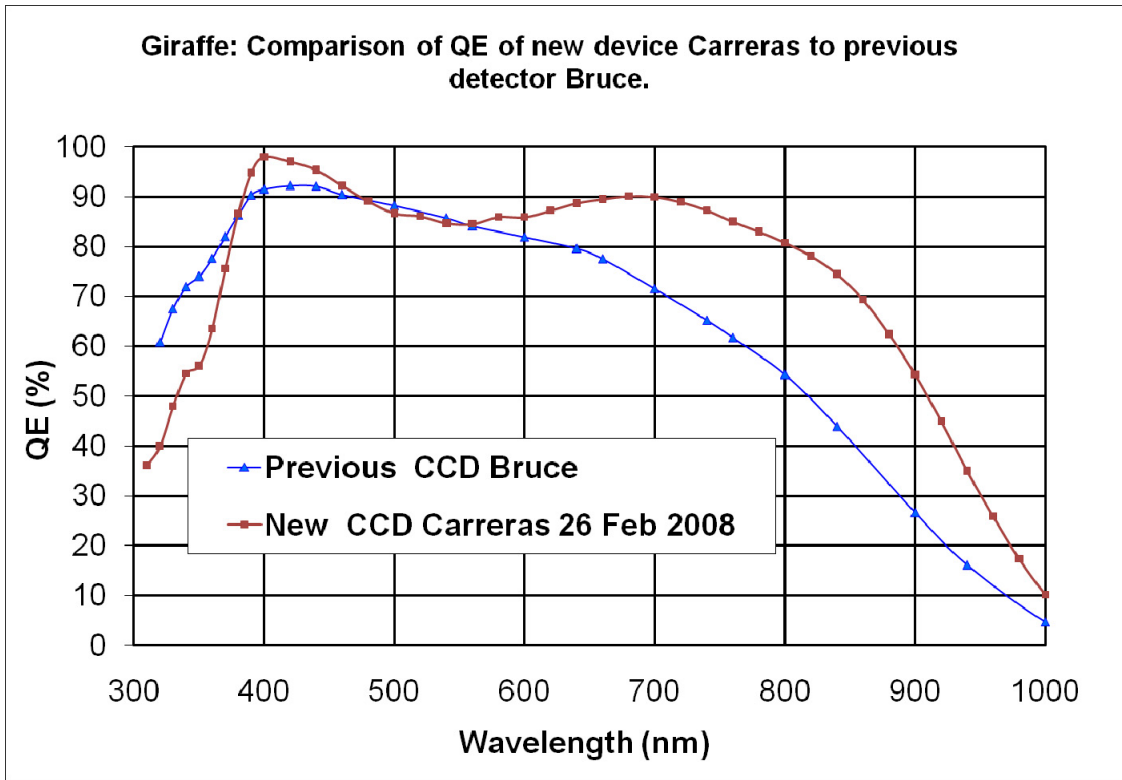
Figure 23: Comparison of QE of upgrade device Carreras to previous detector Bruce
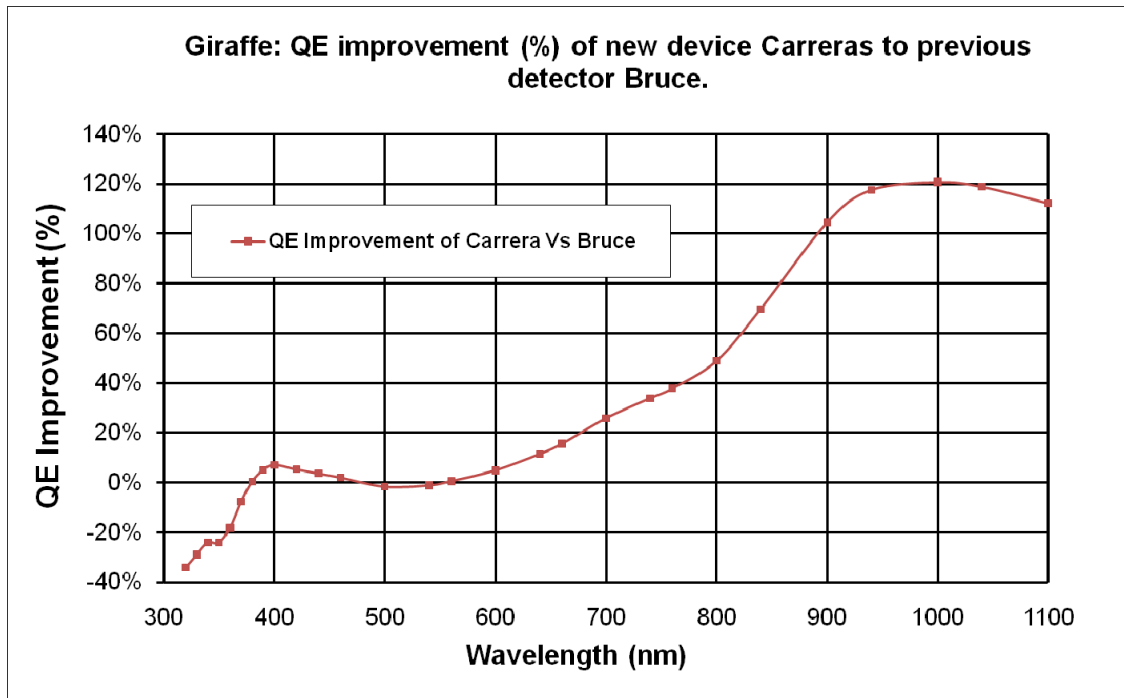
Figure 24: QE improvement (%) of upgrade device Carreras to previous detector Bruce.
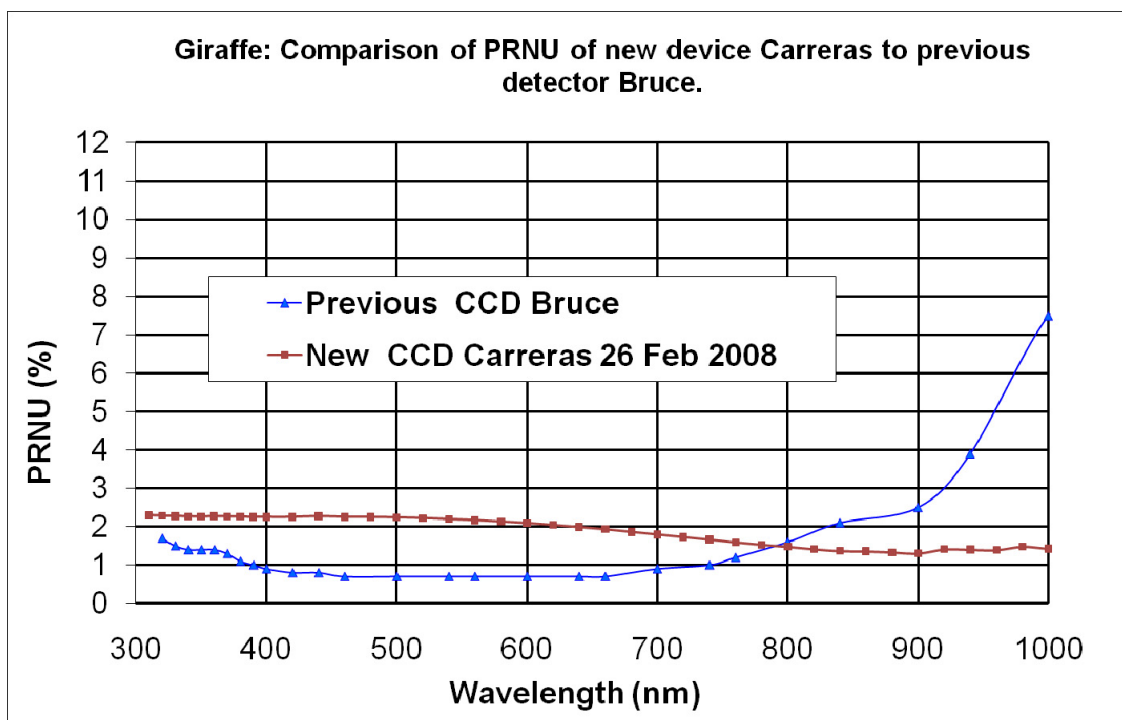
Figure 25: Comparison of PRNU of upgrade device Carreras to previous detector Bruce.

Quantum efficiency and PRNU table (5nm bandwidth).

Table 6: QE and PRNU versus wavelength.

Wavelength	PRNU (%)	QE(%)	Wavelength	PRNU (%)	QE(%)
310	2.3	36	680	1.9	90
320	2.3	40	700	1.8	90
330	2.3	48	720	1.7	89
340	2.3	55	740	1.7	87
350	2.3	56	760	1.6	85
360	2.3	63	780	1.5	83
370	2.3	76	800	1.5	81
380	2.3	87	820	1.4	78
390	2.3	95	840	1.4	75
400	2.2	98	860	1.4	69
420	2.3	97	880	1.3	62
440	2.3	95	900	1.3	54
460	2.3	92	920	1.4	45
480	2.3	89	940	1.4	35
500	2.2	87	960	1.4	26
520	2.2	86	980	1.5	17
540	2.2	85	1000	1.4	10
560	2.2	85	1020	1.4	5
580	2.1	86	1040	1.4	2
600	2.1	86	1060	1.4	1
620	2.0	87	1080	1.4	0
640	2.0	89	1100	1.4	0
660	1.9	90			

8.2.12 Fixed Pattern Noise

During commissioning at Paranal, it was confirmed that the fixed pattern noise of Carreras was not as good as Bruce (see comparison row plots in *Figure 26* at signal level of 50,000 ADU in read out mode

225kpx_1x1_LG). This is in agreement with measurements taken in Garching (see plot in Figure 25 of PRNU versus wavelength).
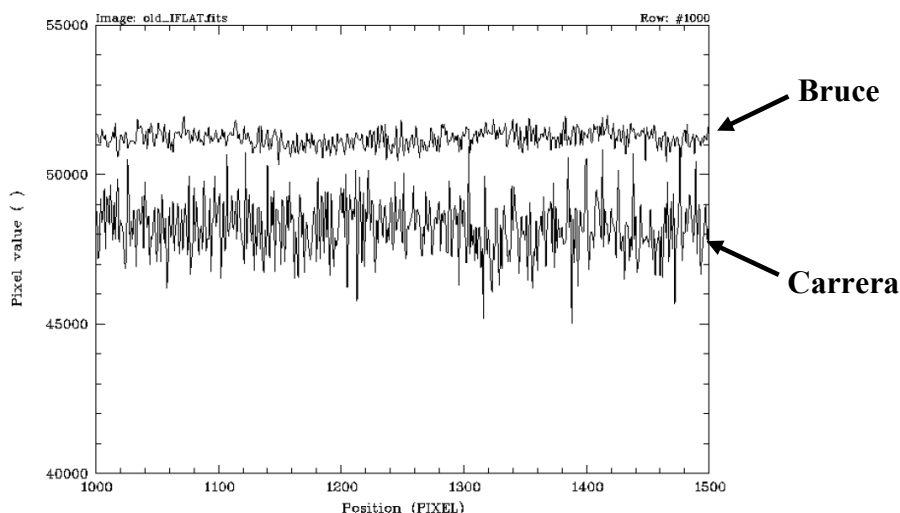
Figure 26: Row plots comparing fixed pattern noise (FPN) using Giraffe broadband flat field lamp at signal level of 50,000 ADU (gain 2.3e/ADU) where the FPN dominates of the previous giraffe detector Bruce (top plot) to the new detector Carreras bottom plot). Note that the fixed noise of Carreras is not as good as Bruce.

Two tests were performed to prove that the FPN can be flat fielded out:

1. A high level (60kADU) flat was divided by low level (6kADU) one. Both first being bias subtracted. The results (*Figure 27*) show no trace of the fixed pattern noise proving that the FPN can be flat fielded out.
2. Fast Fourier Transform was performed on both the high level (60kADU) flat and the high level by low level division. The results (*Figure 28* left) show structure in the spatial frequency domain in the case of the high level flat. However for the division of flats (*Figure 28* right), no structure is visible again proving that the FPN can be flat fielded out.
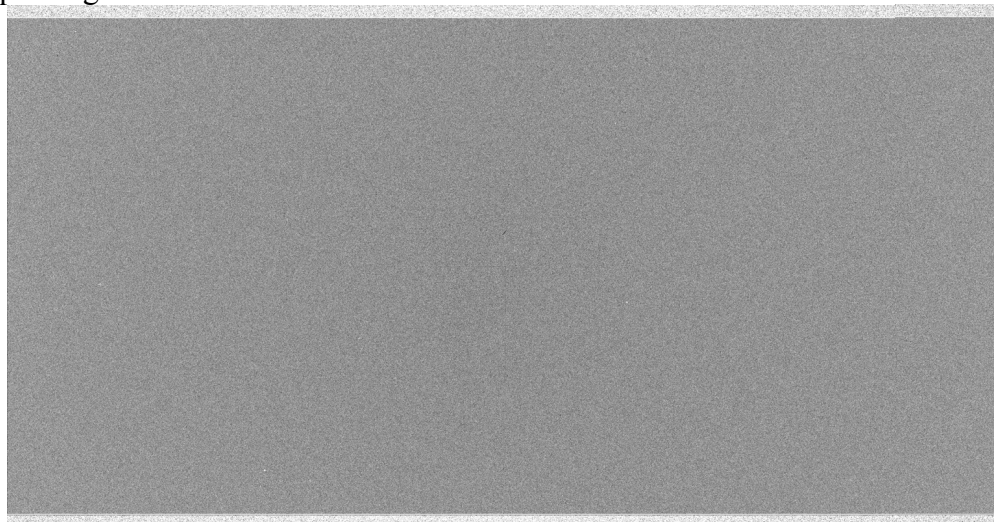
Figure 27: Resulting image of high level (60kADU) divided by low level (6kADU) flat. Both flats were bias subtracted. No pattern or structure of the fixed pattern noise is seen proving that the FPN can be flat fielded out.
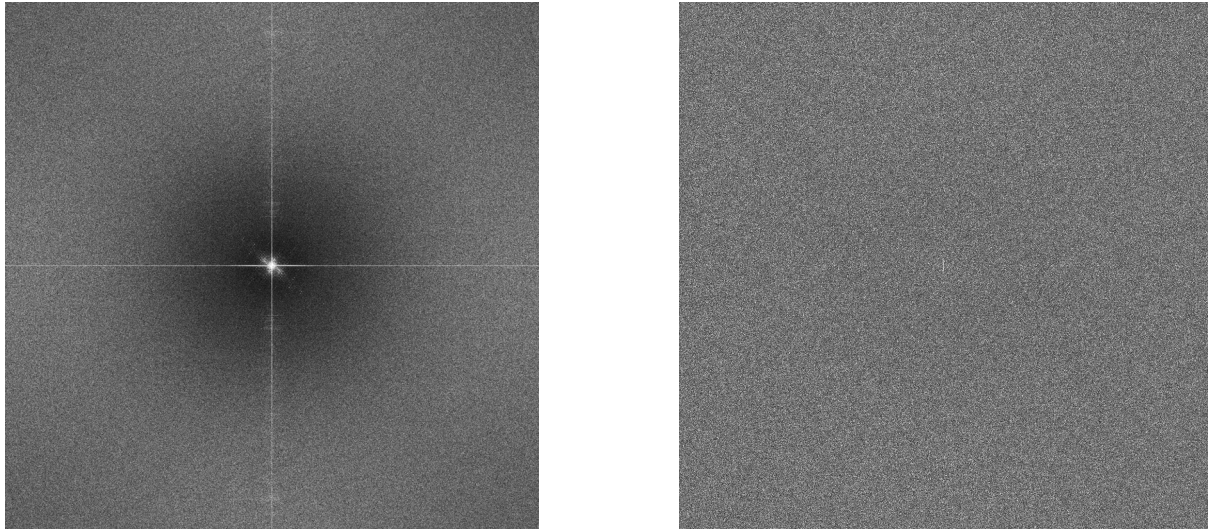
Figure 28: Various FFT images. Left: FFT image of high level (60kADU) flat showing structure in the spatial frequency domain. Right: FFT image of division of high level (60kADU) by low level (6kADU) flat demonstration that all structure (FPN) has been removed.

8.2.13 Variation of Offset Level in a Sequence of Biases

Reinhard Hanuschik noticed that within a sequence of biases the first bias was different to the rest. The question was then asked which bias should be used to generate the master bias. If a master bias is generated from the bias sequence using median filtering, the first bias is ignored as it is different to the rest. Using such generated master bias results in negative DC level in low intensity images and cause problems for the pipeline. The first bias is the correct one and one that should be used to generate the master bias.

To investigate the feature further, several bias sequences were recorded with increasing delays between the biases within the same sequence to determine the delay needed so that all biases are the same as the first bias in a sequence with no delay. Figure 29 contain column plots of the difference between the fifth and first image of a sequence of biases with delays of 0s, 60s, 120s and 180s. To decrease noise, the images were binned and averaged by 20 along a row. Delay of 0s was repeated twice (Figure 30 and Figure 31) days apart to confirm that the first bias is always different. Clearly with delay > 120s, there is little difference between the biases in a sequence and they compare well (not shown but confirmed by analysis) with the first bias in a sequence with no delay.

The conclusion is that for very accurate calibration purposes, master biases should be generated from biases sequences in which the biases are delayed from each other by at least 120s.
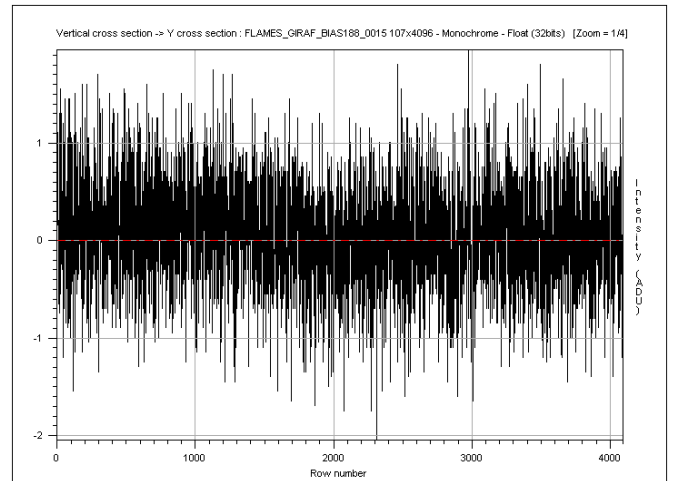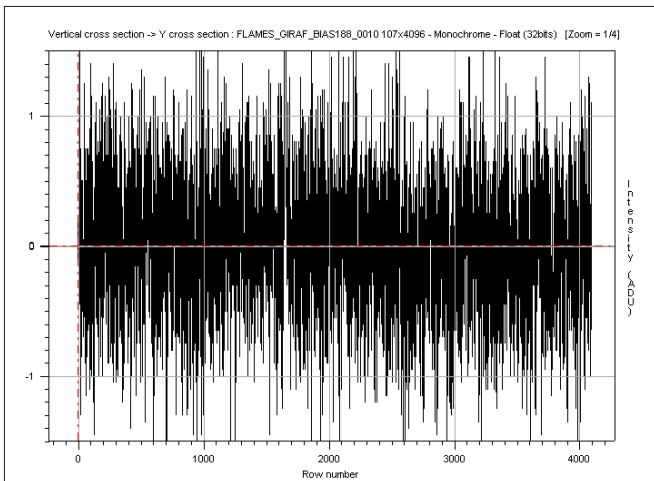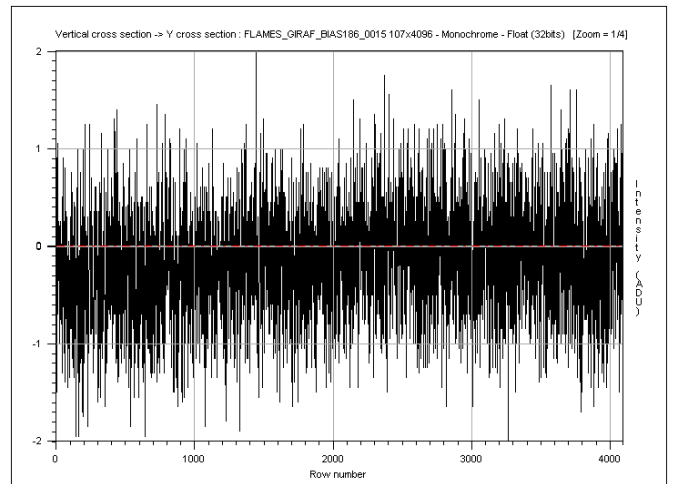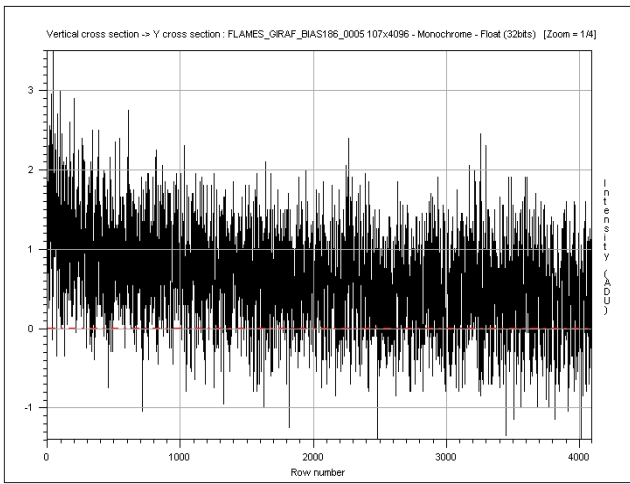
Figure 29: Column plots of the difference between the fifth and first image of a sequence of biases. After subtraction, the images are binned and averaged by 20 along a row. Top left: 0 sec delay between biases; Top right: 60 sec delay between biases; Bottom left:120 sec delay between biases; Bottom right:180 sec

The following sub-sections repeats the analysis but calculates the mean over the image region [200:1000,200:100] and plots this mean as a function of absolute time the bias was taken. Clearly with a gap of < 120sec, the first bias has a different DC level to the rest. The conclusion is the same. For very accurate calibration purposes, master biases should be generated from biases sequences in which the biases are delayed from each other by at least 120s.

Sequence I: 5 biases with no gap between frames
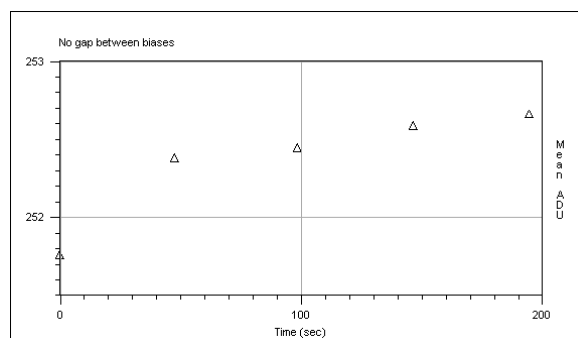
Figure 30: Plots of mean versus time of sequences of 5 biases with no gap between frames.

Exp.time(sec)	Mean	Variance	Filename	Date	Time
0	251.751	3.18267	FLAMES_GIRAF_BIAS186_01	04/07/2008	03:00:14
0	252.373	5.53865	FLAMES_GIRAF_BIAS186_02	04/07/2008	03:01:02
0	252.44	4.37026	FLAMES_GIRAF_BIAS186_03	04/07/2008	03:01:53
0	252.579	4.09436	FLAMES_GIRAF_BIAS186_04	04/07/2008	03:02:41
0	252.651	3.19019	FLAMES_GIRAF_BIAS186_05	04/07/2008	03:03:29

Sequence II: 5 biases with no gap between frames
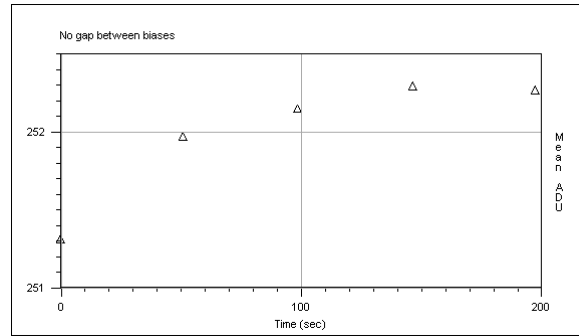
Figure 31: Plots of mean versus time (seconds) of sequence of 5 biases with no gap between frames.

Exp.time(sec)	Mean	Variance	Filename	Date	Time
0	251.304	2.92797	FLAMES_GIRAF_BIAS188_0001	06/07/2008	06:43:57
0	251.966	8.33015	FLAMES_GIRAF_BIAS188_0002	06/07/2008	06:44:48
0	252.137	3.01093	FLAMES_GIRAF_BIAS188_0003	06/07/2008	06:45:36
0	252.284	3.85792	FLAMES_GIRAF_BIAS188_0004	06/07/2008	06:46:24
0	252.261	3.04499	FLAMES_GIRAF_BIAS188_0005	06/07/2008	06:47:14

Note that the average offset level does vary between Figure 30 and Figure 31 but always the first bias is different to the subsequent.

Sequence of 5 biases with 30-sec gap between frames
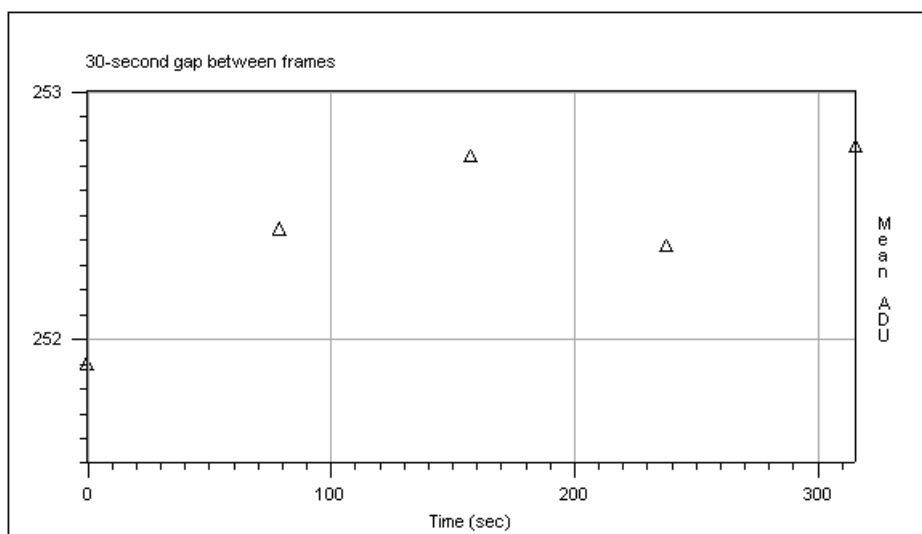
Figure 32: Plots of mean versus time (seconds) of sequence of 5 biases with 30-second gap between frames.

Sequence of 5 biases with 60-sec gap between frames
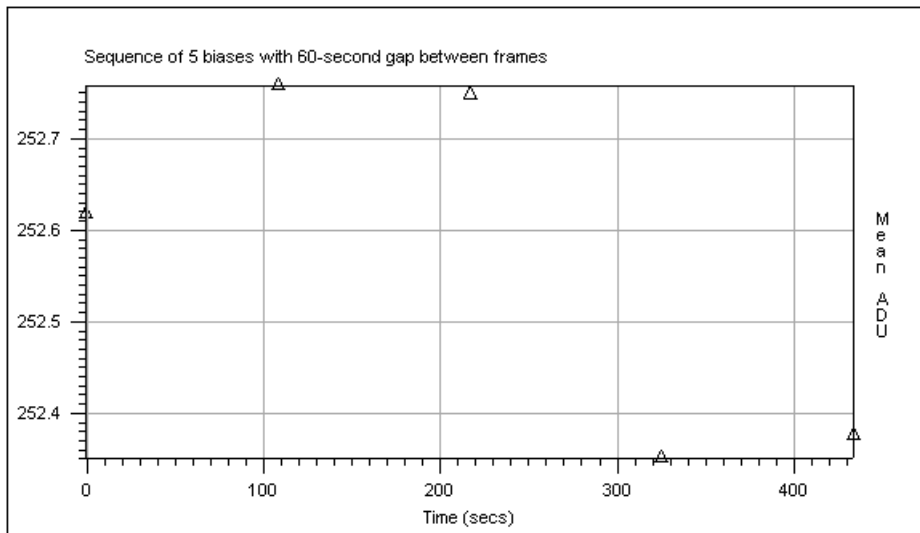
Figure 33: Plots of mean versus time (seconds) of sequence of 5 biases with 60-second gap between frames.

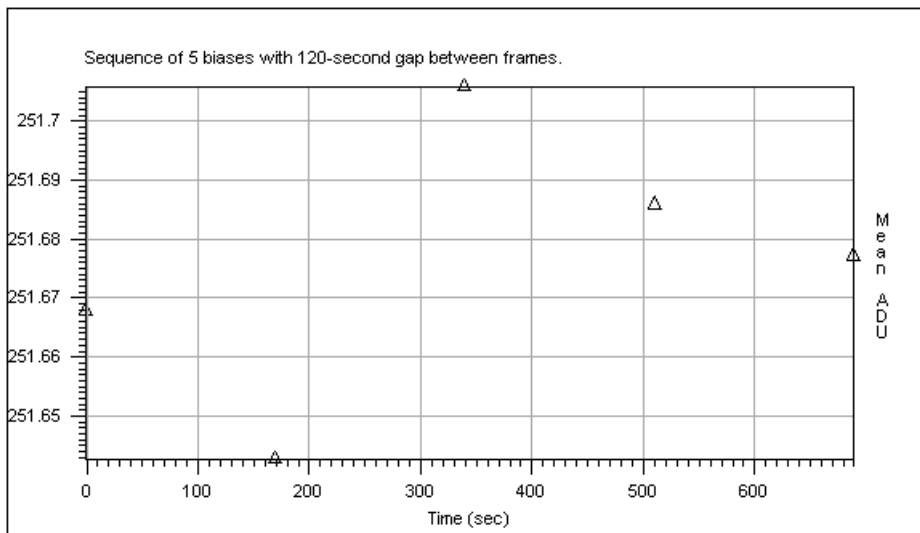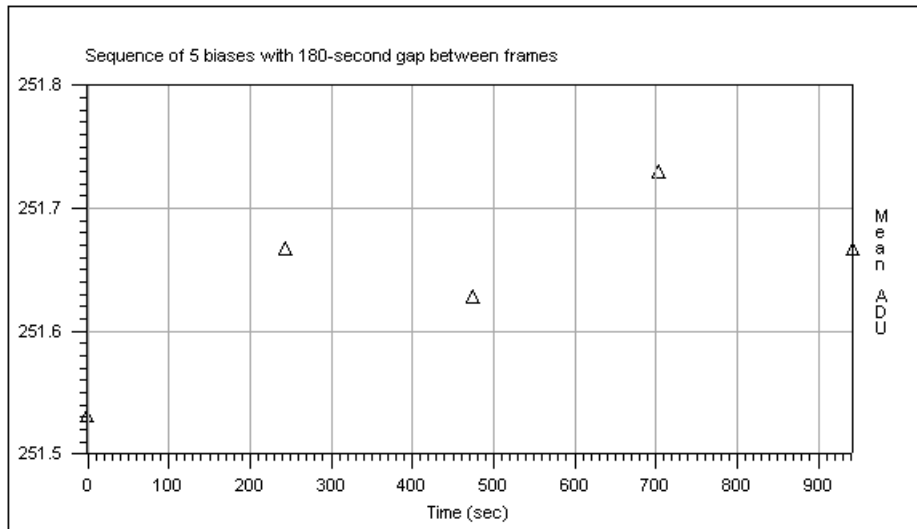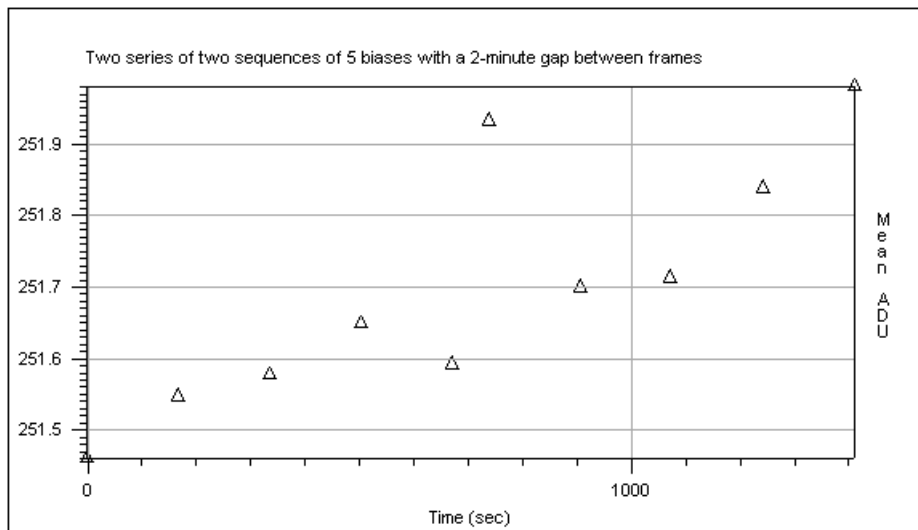## Sequence of 5 biases with 120-sec gap between frames

Figure 34: Plots of mean versus time (seconds) of sequence of 5 biases with 120-second gap between frames.

Sequence of 5 biases with 180-sec gap between frames

Figure 35: Plots of mean versus time (seconds) of sequence of 5 biases with 180-second gap between frames.

Two sequences of 5 biases with a 2-minute gap between frames

Figure 36: Plots of mean versus time of two series of two sequences of 5 biases with a 2-minute gap between frames.

Exp.time(sec)	Mean	Variance	Filename	Date	Time
0	251.459	2.93054	FLAMES_GIRAF_BIAS192_0003	10/07/2008	16:30:44
0	251.547	37.0388	FLAMES_GIRAF_BIAS192_0004	10/07/2008	16:33:31
0	251.577	2.94952	FLAMES_GIRAF_BIAS192_0005	10/07/2008	16:36:21
0	251.647	2.97048	FLAMES_GIRAF_BIAS192_0006	10/07/2008	16:39:08
0	251.591	2.95646	FLAMES_GIRAF_BIAS192_0007	10/07/2008	16:41:55
0	251.932	14.3194	FLAMES_GIRAF_BIAS192_0008	10/07/2008	16:43:04
0	251.699	2.97377	FLAMES_GIRAF_BIAS192_0009	10/07/2008	16:45:51
0	251.712	2.96613	FLAMES_GIRAF_BIAS192_0010	10/07/2008	16:48:38
0	251.837	2.99099	FLAMES_GIRAF_BIAS192_0011	10/07/2008	16:51:28
0	251.979	3.0207	FLAMES_GIRAF_BIAS192_0012	10/07/2008	16:54:16

8.3 Opto-mechanical requirements

The flatness tolerances are still based on a maximum allowable defocus blur of 10 μm with a target of 5 μm (note that the optics will deliver 80% of the energy within a circle of 15 - 20 μm).

Table 7: Comparison of opto-mechanical requirements required and achieved.

	Requirements	Results
Item	detector (EEV 2K x 4K chip)	detector (Carreras)
Optical field size	Ø68 mm	Fulfilled
BFD[1]	$2\ ^{+0.03}_{-0.03}$ mm	Fulfilled
De-centering[2]	< 0.5 mm	Fulfilled
P-V flatness	< 36 μm Goal : 18 μm [3]	Fulfilled

1. *The distance of the average CCD surface to the reference flange (mounting surface of field lens holder)*
2. *The distance between the optical center of the chip (not taking into account possible overscan pixels) and the mechanical axis of the dewar.*
3. *The distance of two planes, parallel to the reference flange, between which the sensitive surface of the chip or mosaic is contained. Applies to optical field size only.*

9 System pictures

Location	Activity	Date	Figures
Garching	Shipment received	25-Mar-2008	
	Unpacked and Cryostat disassembled	26-Mar-2008	Figure 37
	Reused parts cleaned: • CCD Mount was cleaned in ultra sonic alcohol bath, dried, then vacuum baked for two days. • Metal parts of flange were wiped with alcohol then air dried with compressed air. No baking as no one knew (i.e. what "o" rings and greases are inside) to what temperature it could be baked.	27-Mar-2008	
	Cryostat re-assembled and Alignment	28-Mar-2008	Figure 38
	Vacuum leak tested, Pumped and Baked	28-Mar-2008 to 01-Apr-2008	
	CCD Characterized	02-Apr-2008 to 07-Apr-2008	
	Contamination detected after dark tests	07-Apr-2008	Figure 39
	Diagnostic that contamination is ice (water) on CCD surface	08-Apr-2008 to 09-Apr-2008	Figure 40
	Cryostat warmed up, leak tested and baked to get rid of contamination	10-Apr-2008 to 15-Apr-2008	
	Cooled down to check progress of baking (no ice). Performance of CCD confirmed with Giraffe video and bias board.	16-Apr-2008	
	Cryostat warmed up and baking continued	17-Apr-2008 to 21-Apr-2008	
	Cryostat packed up and shipped to Paranal by container	21-Apr-2008	
Paranal	Cryostat arrives at Paranal	28-Apr-2008	
	Cryostat pumped and baked at 30ºC	28-Apr-2008 to 2-May-2008	
	Cryostat installed on Giraffe spectrograph on UT2, cabled and cooled down.	2-May-2008 to 3-May-2008	Figure 41 Figure 42
	CCD performance confirmed.	4-May-2008 to 5-May-2008	

9.1 Garching

Packing Box

Items Received
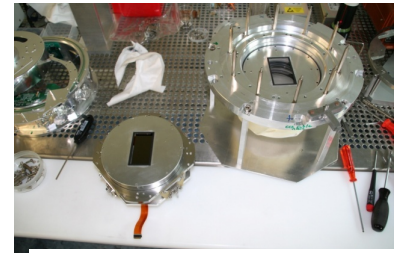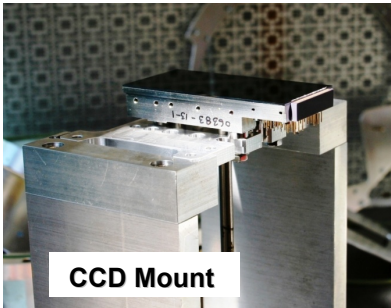

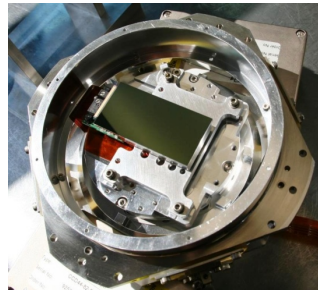**Reused CCD Mount and Flange**
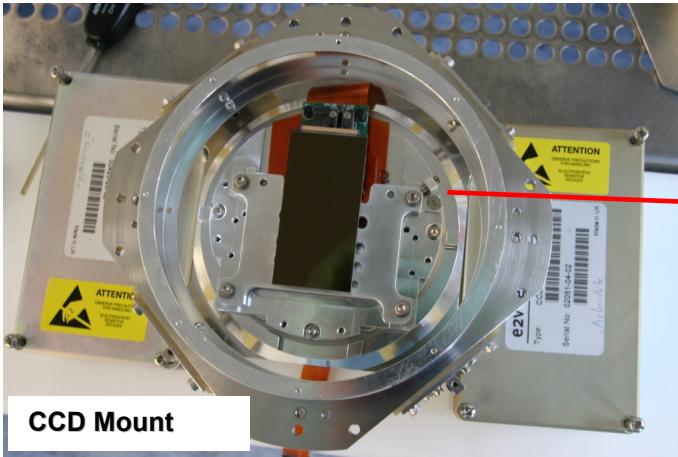
CCD Mount

Mechanical Stop keeps X/Y alignment

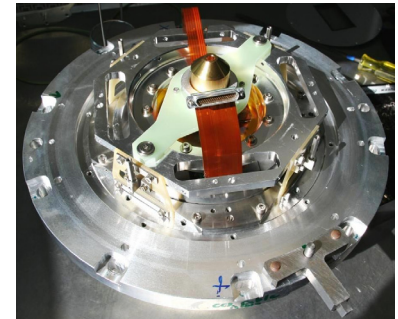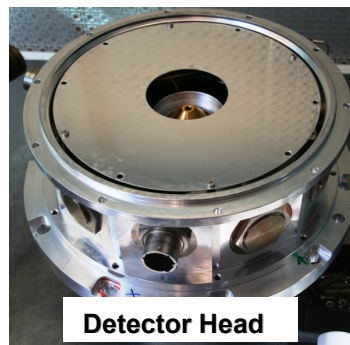*Figure 37: Disassembly in Garching 26th Mar 2008. Shipment received 25th Mar 2008.*
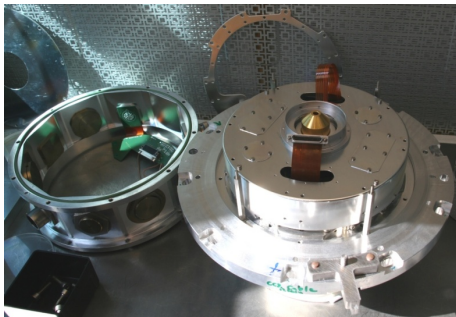

CCD Mount

CCD Mounted

**CCD Mount and Flange**

Detector Head

Complete Cryostat

Figure 38: Re-assembly of cryostat in Garching 28th Mar 2008.

9.2 Contamination

Contamination (see Figure 39) was noticed five days after first cool down with Giraffe flange installed. To prove that the contamination was water, the temperature of the CCD was varied from 160K (ice) to 180K (no ice) at constant pressure (10-5 mbarr) to determine the point of sublimation. The contamination was found to have the same sublimation point temperature of ~ 170K as water (see Figure 40 for phase diagram of water-ice-steam) thus is believed to be the result of water trapped in the anodizing of the flange. The cryostat was baked (sieve heater turned on and whole cryostat raised to 30ºC by heating the room) for several days to remove the contamination. The baking was continued in Paranal for four days until the system was installed. No contamination was observed during the commissioning run.
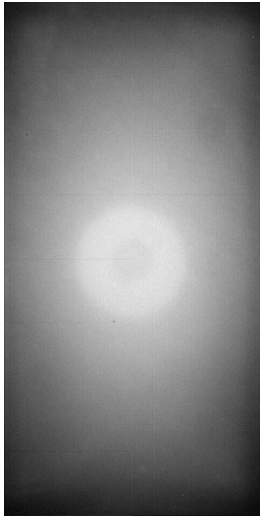
Flat field image showing no contamination when first cooled
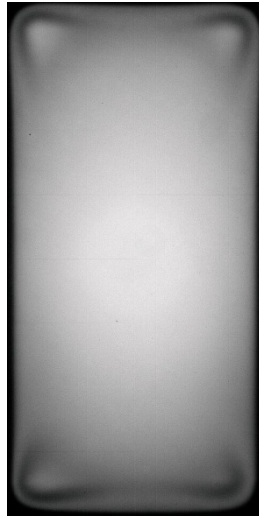
Flat field image showing contamination

Photo of CCD showing contamination

Figure 39: Images and photo showing contamination observed on CCD. Left: Flat field image showing no contamination when first cooled. Middle: Flat field image showing contamination. Right: Photo of CCD looking through lens showing contamination. Note thicker layer of ice around edge of CCD.
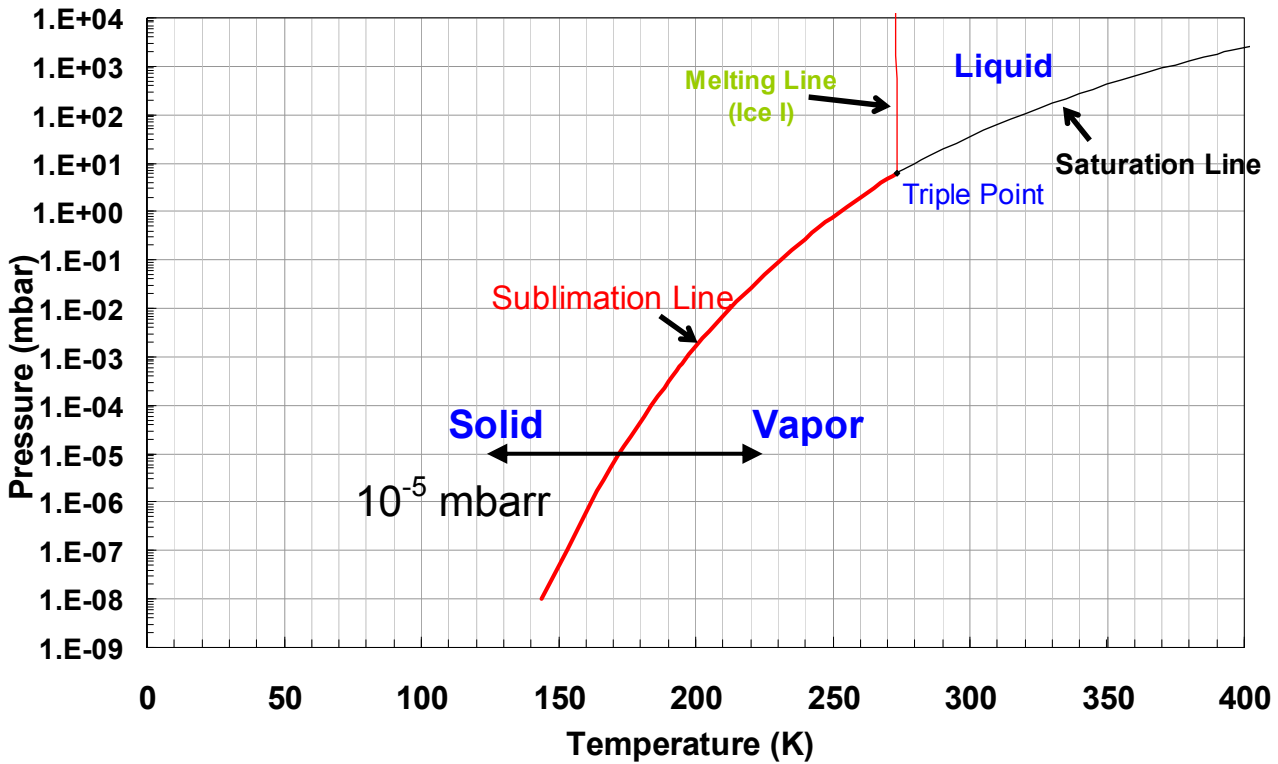
Figure 40: Phase diagram of water-ice-steam. To prove that the contamination is water, the temperature of the CCD was varied from 160K (ice) to 180K (no ice) at constant pressure (10-5 mbarr) to determine the point of sublimation. The contamination has the same sublimation point of ~ 170K as water thus is highly likely water trapped in the anodizing of the flange
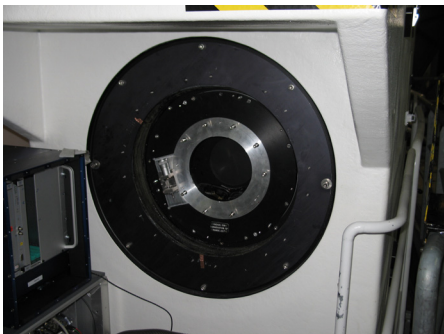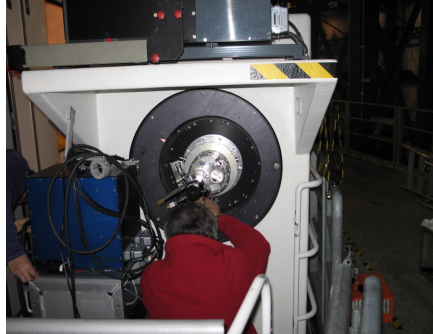
9.3 Paranal
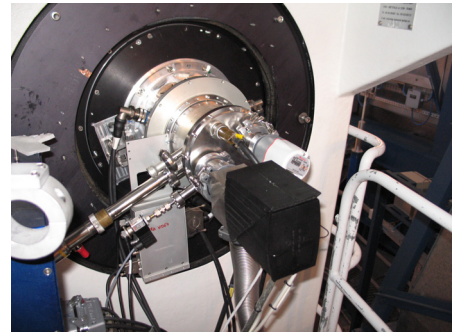

Cryostat Ready for mounting
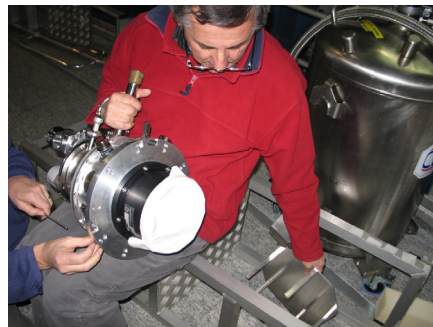
Lens cover removed

Lens in good order

Mounting flange

Cryostat being mounted

Cryostat Cabled

Figure 41: Mounting cryostat at Paranal 2-3 May 2008.

FIERA Front

FIERA Rear

Cryogenic controller

Figure 42: Photos of FIERA and Cryogenic controller.